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TITLE: DISPLAY SYSTEM WITH MULTIPLEXED PIXELS

Abstract Paragraph:
A display matrix is provided comprising a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel and at least partially positioned outside of a footprint of the pixel, the display circuit including a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time.

Cross Reference to Related Applications Paragraph:
[0001] This application is a continuation-in-part of "Display System Having Multiple Memory Elements Per Pixel," application Ser. No. 09/079,684; Filed: May 15, 1998 and "Display System With Local Decoding," application Ser. No. <Atty. Docket No. 17542-736>; Filed: May 13, 1999 which is incorporated herein by reference.

Summary of Invention Paragraph:
[0003] The invention generally relates to a display system for producing an image and more specifically to a display system for providing a sequentially produced composite image.

Summary of Invention Paragraph:
[0005] A continuing objective in the field of electronics is the miniaturization of electronic devices. Most electronic devices include an electronic display. As a result, the miniaturization of electronic displays is critical to the production of a wide variety of compact electronic devices.

Summary of Invention Paragraph:
[0006] The purpose of an electronic display is to provide the eye with a visual image of certain information. This image may be provided by constructing an image plane composed of an array of picture elements (or pixels) which are independently controlled as to the color and intensity of the light emanating from each pixel. The electronic display is generally distinguished by the characteristic that an electronic signal is transmitted to each pixel to control the light characteristics which determine the pattern of light from the pixel array which forms the image.

Summary of Invention Paragraph:
[0007] Two examples of electronic displays are the cathode ray tube (CRT) and the active-matrix liquid crystal display (AMLCD). There are other electronic displays, but none are so well developed as the CRT and AMLCD which are used extensively in computer monitors, televisions, and electronic instrument panels. The CRT is an emissive display in which light is created through an electron beam exciting a phosphor which in turn emits light visible to the eye. Electric fields are used to scan the electron beam in a raster fashion over the array of pixels formed by the phosphors on the face plate of the electron tube. The intensity of the electron beam is varied in an analog (continuous) fashion as the beam is swept across the image plane, thus creating the pattern of light intensity which forms the visible image. In a color CRT, three electron beams are simultaneously scanned to

independently excite three different color phosphors respectively which are grouped into a triad at each pixel location.

Summary of Invention Paragraph:
[0008] In contrast to the emissive type displays such as the CRT, an AMLCD display utilizes a lamp to uniformly illuminate the image plane which is formed by a thin layer of liquid crystal material laminated between two transparent conductive surfaces which are comprised of a pattern of individual capacitors to create the pixel array. The intensity of the illumination light transmitted through each pixel is controlled by the voltage across the capacitor, which is in turn controlled by an active transistor circuit connected to each pixel. This matrix of transistors (the active matrix) distinguish the AMLCD from the passive matrix liquid crystal devices which are strictly an array of conductors controlled by transistors external to the image area usually in the periphery of the matrix. The ability of each transistor to control the characteristics of just one pixel allows for the higher performance found in AMLCD displays in contrast to the passive arrays.

Summary of Invention Paragraph:
[0010] In most displays, the electronic activation of the image must be continuous or persistent through repetition. In the CRT and emissive displays in general, a constant or highly repetitive source of energy must be applied to the pixel to create photon emission. Phosphor decay times are typically a few milliseconds. Similarly, the capacitors in the AMLCD array lose their charge through leakage and accurate grayscale levels are lost. Furthermore, many liquid crystal materials exhibit ion migration and must be reversed in polarity with each refresh cycle. In general, displays with limited persistence must be refreshed frequently to avoid noticeable brightness variation known as flicker. On the other hand, displays with substantial persistence cannot display moving images without ghost images. Refreshing the image of most displays requires repeated transmission of the image data to the display, either from the broadcast source or from a storage device.

Summary of Invention Paragraph:
[0011] Not all electronic products which contain an electronic display have memory for storing the data which is to be displayed. For instance, a television must activate the CRT display in real time as the broadcast signal is received unless a VCR or similar storage medium is employed. In computers, data is transmitted and stored digitally. Moreover, in portable electronics devices, size and power constraints require the use of semiconductor memory which stores data only in digital format. In digital electronic products, it is typical that a display controller is incorporated to receive and store the bit mapped image to be displayed and then to transfer that data to the display in a series of image frames at a rate high enough to look smooth to the eye. The semiconductor memory storing the image bits is called the frame buffer, and the rate at which the data is refreshed on the display is called the frame rate.

Summary of Invention Paragraph:
[0012] It is an advantage in many applications to display large amounts of information requiring more and more resolution in the display. High resolution displays may contain hundreds of thousands of pixels. As an example, the Super VGA (SVGA) display resolution consists of 480,000 pixels. With a simple monochrome image and no grayscale, the frame storage is only equal to the approximately one-half megabit frame size. However, were the image to be full 24 bit depth color (i.e., 3 colors and 8 bits of grayscale per color), the frame storage would approach 12 megabits. At the frame rates which are common today for high performance displays, at least 60 frames per second and up to 85 frames per second, as many as one gigabits per second must be transferred from the frame buffer to the display. The state of semiconductor technology at present limits clock speeds to a level well below such transfer rates and parallel interfaces of 16 to 32 bit widths are typical in high performance displays.

Summary of Invention Paragraph:
[0013] It is a characteristic of analog displays that when the image data is stored in semiconductors, the digital information is converted to analog in a digital-to-analog converter (DAC) at the interface of the display. The digital representation of a pixel at the high standard of 8 bits of grayscale allows the creation of 256 separate shades per color (16 million distinct colors). In high performance displays, multiple DAC channels are required to provide the bandwidth of data transfer required.

Summary of Invention Paragraph:
[0014] As was noted above, most displays must be frequently rewritten to maintain an image. In the case of both CRT and AMLCD displays, data is being rewritten to one part of the display area while the rest of the array continues to display the prior image frame. This property is particular to monochrome displays and to color images are created from a composite of spatially separated sub-pixels. There is a clear advantage to writing and displaying data at the same time allowing each function to make maximum utilization of time allowed for each frame.

Summary of Invention Paragraph:
[0015] Once data corresponding to an image is transferred to a display via electronic signals, there is an advantage to the display device being able to maintain the image unless a portion of the image must be altered to provide motion to the image. The amount of data written to the display in each subsequent frame can be substantially reduced if the writing operation is organized to be random, such as to write data to any location in the array and only to those locations where the data is changing for reasons that the image is moving or for reasons the array is reused sequentially to create a composite image. To achieve this end however, pixel locations which are not being rewritten must be able to store data and continually display it.

Summary of Invention Paragraph:
[0017] Similarly, in an active matrix display a multiplicity of transistors may be provided in correspondence to each pixel such that a static memory (SRAM) cell (typically four or six transistors) can be utilized to activate each pixel. There are several advantages to static memory such as the on-state output voltage always being at the rail voltage, the low activation current, no voltage decay, and sufficient signal to noise to read from the memory cells any stored data. However, because a static memory cell is itself bistable, the pixel activation will provide no analog grayscale.

Summary of Invention Paragraph:
[0018] In general, displays with no analog response fall into two categories. Those displays with an extremely fast response in relation to the time divisions of the on-off cycles (as is typical of MEMS devices) can achieve grayscale through pulse width modulation. Those displays with a relatively slow response time in relation to on-off cycles (as is typical of liquid crystal devices) can achieve grayscale through a root mean square (RMS) voltage level based on the average time-voltage product. In both cases however, there is a disadvantage in comparison to analog grayscale methodologies, that being the loss of parallelism of the data transfer of the grayscale bits. Data transfer rates from frame buffers to a binary display device can be significantly higher than an analog display.

Summary of Invention Paragraph:
[0019] In the particular case of miniaturization of high resolution electronic displays, there is an advantage to reducing the size of the pixels which comprise the display. The need for such small devices has led to the development of a category of miniature displays often described as microdisplays with pixel sizes as small as 10 microns. In order to achieve this pixel resolution, active matrix devices have been developed utilizing silicon wafer fabrication of CMOS devices as opposed to thin-film transistors fabricated on a glass or quartz substrate. Single

crystal silicon design rules are many times smaller than poly-silicon resulting in transistor sizes to easily fit microdisplay geometries. With the exception of techniques to separate the single crystal transistors from the silicon substrate utilizing lift-off technology, CMOS based active matrix displays are inherently opaque, and therefore must be reflective rather than transmissive like the poly-silicon devices. Thin film transistor (TFT) based transmissive devices are also opaque as transistors and interconnection lines, and optical efficiencies are very low for high resolution TFT displays.

Summary of Invention Paragraph:
[0021] The pixel sizes are also small relative to the size of color filters used in TFT AMLCD displays to create color triads for each pixel. There is a significant advantage to creating color through the sequential use of the entire array to create an image specific to each of the three prime color components. Through the utilization of separate light emitting diodes of each prime color to illuminate the display, the diodes can be turned rapidly on and off to correspond to the particular color component being displayed by the array at that moment. This method of color creation is called field sequential color wherein each color field is sequentially illuminated by the appropriate diode.

Summary of Invention Paragraph:
[0022] An important limitation of the field sequential color method is that data for the next color field cannot be written while the current color field is being illuminated. As a result, the time available to write to the display is limited and must be substantially less than the time allowed to illuminate each particular field's color.

Summary of Invention Paragraph:
[0023] Because at least three different color images need to be displayed at a rate faster than can be resolved by the eye, the field sequential color method at least triples the frame rate required as compared to a monochrome display.

Summary of Invention Paragraph:
[0024] A need exists for a display system which can overcome the various above-described limitations of prior art display systems and be able to produce a high resolution field sequential color image which is not limited by the frame transfer rate limitations of existing display matrices. The display system should also be adaptable for use as a microdisplay.

Summary of Invention Paragraph:
[0025] A significant aspect of a compact electronic device is its portability. It is impractical and disadvantageous for a compact electronic display to rely on an external power source. Rather, compact electronic displays must rely on an internal battery for energy. It is important to the usefulness and reliability of the electronic display that the display be energy efficient so that the battery life of the display is optimized. A need thus exists for an energy efficient display for use in portable electronic devices.

Summary of Invention Paragraph:
[0026] These and other advantages are provided by the display system of the present invention.

Summary of Invention Paragraph:
[0027] A display matrix is provided for forming a composite image from a series of sub-images. In general, the display matrix includes a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel. Each display circuit includes a plurality of memory cells, and a selector for outputting to the pixel data from one memory cell at a time.

Summary of Invention Paragraph:
[0028] According to one aspect of the display matrix of the present invention, a plurality of memory cells in the display circuit are continuously electrically connected to the selector of the display circuit at the same time. As a result, there is no need to address a particular memory cell to a particular selector. This may be accomplished, for example, by the display circuit including separate conductive elements for each memory cell in the display matrix which electrically connects a memory cell to the selector in the display circuit.

Summary of Invention Paragraph:
[0029] According to another aspect of the display matrix of the present invention, the display matrix is formed on a substrate having a plurality of regions where each region includes a memory circuit with a plurality of memory cells, and a selector electrically connected to the plurality of memory cells in the region. The substrate may be any material on which the display circuit may be attached or formed. In a preferred embodiment, the substrate is a semiconductor, such as silicon, on which the display circuits are formed by one or more of a variety of methods known in the art.

Summary of Invention Paragraph:
[0030] According to this aspect, the memory cells are physically interdispersed among the selectors within the plurality of display elements. In this regard, the memory associated with the display matrix is integrated into the display matrix as opposed to be external to the display matrix and the selectors.

Summary of Invention Paragraph:
[0031] According to the present invention, at least a portion of the display circuits of the display matrix include at least 2 memory cells per display circuit. In one embodiment, at least a portion of the display circuits of the display matrix include at least 3 memory cells per display circuit. The display matrix may optionally include 4-18 or more memory cells per display circuit, depending on a variety of factors which will be discussed herein.

Summary of Invention Paragraph:
[0032] In a preferred embodiment, the display matrix has sufficient memory such that data can be transferred to the display matrix for one sub-image while a different sub-image is displayed. The display matrix may also have sufficient memory to display two or more different sub-images without having to write to the memory cells between displaying the different sub-images. The plurality of memory cells in each circuit can represent different bits of a digital grayscale value. It is possible to vary the digital grayscale value significance of a particular memory cell image to image and field to field. The plurality of memory cells in each circuit can represent bits of different color fields.

Summary of Invention Paragraph:
[0033] In one embodiment, the display circuit can be operated in a field sequential color (FSC) mode without having to write to the memory cells between displaying different fields. This enables the display matrix to not need an external frame buffer. The display matrix may optionally be configured to be operated in a field sequential color (FSC) mode without having to write to the memory cells between displaying different fields.

Summary of Invention Paragraph:
[0035] In one embodiment, the display matrix is sized to form a microdisplay. According to this variation, the pixels in the plurality of display elements may form a source object having an area equal to or less than about 400 mm.sup.2 and preferably between about 20 mm.sup.2 and 100 mm.sup.2. The pixels of the display matrix preferably have an area less than about 0.01 mm.sup.2 and more preferably between 50 .mu.m.sup.2 and 500 .mu.m.sup.2.

Summary of Invention Paragraph:
[0036] The present invention also relates to a display system which includes a display matrix according to the present invention and peripheral control circuits for controlling read and write operations to the memory cells. The display system may also include an illumination source for illuminating the pixels. In one embodiment, the display includes a light emitting mechanism provided at each pixel. The display system may also include a light modulating mechanism, such as a liquid crystal material, provided at each pixel.

Summary of Invention Paragraph:
[0037] The display system may optionally further include logic for reading, inverting and rewriting data stored in the memory cells to provide a refresh cycle, a processor for reading, modifying, and rewriting data stored in the memory cells to compose a bit mapped image without the need of an external frame buffer, control circuits for reading, modifying, and rewriting data stored in the memory cells to provide a cursor function. The peripheral control circuits may also serve to read, move, and rewrite data stored in the memory cells to provide a scroll function.

Summary of Invention Paragraph:
[0038] The display system may also include an illumination source capable of providing a plurality of different color illumination to the pixels, the particular color illumination provided to the pixels being coordinated by the peripheral control circuits with the read and write operations to the memory cells. Two, three or more different colors of illumination may be provided. The illumination source preferably provides at least three different colors of illumination.

Summary of Invention Paragraph:
[0039] The display matrices and display systems of the present invention may be used in a display component of a variety of electronic devices. Examples of such devices include, but are not limited to portable computers, personal communicators, personal digital assistants, modems, pagers, video and camera viewfinders, mobile phones, and television monitors. In one particular embodiment, the display matrices and display systems of the present invention are used in combination with one or more magnification optics to form a virtual image display system.

Summary of Invention Paragraph:
[0040] The present invention also relates to methods of using the display matrices and display systems of the present invention to produce composite images as described herein.

Summary of Invention Paragraph:
[0041] The present invention also relates to various display matrix embodiments relating to designing an effective layout for a display matrix having a plurality of memory cells per pixel.

Summary of Invention Paragraph:
[0042] In one embodiment, a display matrix is provided which comprises a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel and at least partially positioned outside of a footprint of the pixel, the display circuit including a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time.

Summary of Invention Paragraph:
[0044] Also according to this embodiment, a first display element may have a display circuit of second display element at least partially positioned inside the footprint of the pixel of the first display element.

Summary of Invention Paragraph:

[0045] Also according to this embodiment, the display matrix may further include a data line electronically connected to both a first display circuit of a first display element and a second display circuit of a second display element, the data line enabling reading from and writing to the first and second display circuits.

Summary of Invention Paragraph:
[0046] Also according to this embodiment, the display matrix may further include two or more data lines, each data line electronically connected to both a first display circuit of a first display element and a second display circuit of a second display element, the data line enabling reading from and writing to the first and second display circuits. The two or more data lines may comprise a first data line which carries a bit signal, and a second data line which carries a bit bar signal.

Summary of Invention Paragraph:
[0047] In another embodiment, a display matrix is provided which comprises a first display element including a first pixel, and a first display circuit including a plurality of memory cells electrically connected to the first pixel; a second display element including a second pixel, and a second display circuit including a plurality of memory cells electrically connected to the second pixel, the second display circuit being at least partially positioned within a footprint of the second pixel and within a footprint of the first pixel.

Summary of Invention Paragraph:
[0048] According to this embodiment, the first display circuit may be at least partially positioned within the footprint of the second pixel, the display matrix optionally including a set of data lines is electronically connected to the first display circuit and the second display circuit, the set of data lines enabling reading to and writing from the first display circuit and the second display circuit.

Summary of Invention Paragraph:
[0049] In another embodiment, a virtual image display system is provided comprising: a display matrix including a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel and at least partially positioned outside of a footprint of the pixel, the display circuit including a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time; peripheral control circuits for controlling read and write operations to the memory cells; and one or more magnification optics for magnifying the sub-images formed by the display matrix.

Summary of Invention Paragraph:
[0050] According to this embodiment, the virtual image display system may optionally include a light emitting mechanism provided at each pixel, a light modulating mechanism provided at each pixel, and/or an illumination source for illuminating the pixels.

Summary of Invention Paragraph:
[0051] In another embodiment, a virtual image display system is provided comprising: a display matrix comprising a first display element including a first pixel, and a first display circuit including a plurality of memory cells electrically connected to the first pixel, a second display element including a second pixel, and a second display circuit including a plurality of memory cells electrically connected to the second pixel, the second display circuit being at least partially positioned within a footprint of the second pixel and within a footprint of the first pixel; peripheral control circuits for controlling read and write operations to the memory cells; and one or more magnification optics for magnifying the sub-images formed by the display matrix.

Summary of Invention Paragraph:
[0052] In yet another embodiment, a method is provided for reducing the number of address lines in a pixel-based display system, the method comprisng: electrically connecting a plurality of display circuits to a plurality of pixels each having a footprint, the plurality of display circuits controlling the operation of the plurality of pixels; positioning the plurality of display circuits relative to the plurality of pixels such that at least a portion of the plurality of display circuits are not entirely positioned within the footprint of a single pixel; and connecting data lines to the plurality of data circuits to read and write data to the plurality of data circuits.

Summary of Invention Paragraph:
[0053] According to another embodiment, a display matrix is provided having a plurality of pixels and a plurality of display circuits which control operation of the plurality of pixels. The display matrix comprises two or more groups of display circuit clusters, each cluster including one or more display circuits electronically connected to a first address line and one or more display circuits electronically connected to a second address line different from the first address line; and an address decoder electronically connected to the display circuits in the cluster which selects between the one or more display circuits electronically connected to the first address line and the one or more display circuits electronically connected to the second address line.

Summary of Invention Paragraph:
[0054] According to this embodiment, the address decoder may be connected to one or more sub-address lines which selects one or more display circuits in the cluster. Also according to this embodiment, the address decoder may be connected to an enable line which signals an enabled/disabled state to the address decoder. Also according to this embodiment, the matrix may include display circuit clusters electronically connected to at least four address lines, the address decoder selecting between the at least four address lines. Also according to this embodiment, each display circuit may comprise a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time.

Summary of Invention Paragraph:
[0055] According to another embodiment, a display matrix is provided which comprises: a plurality of display circuits which control operation of a plurality of pixels, the plurality of display circuits including a first group of display circuits including at least one display circuit electronically connected to a first address line and at least one display circuit electronically connected to a second address line different from the first address line, a second group of display circuits including at least one display circuit electronically connected to a third address line and at least one display circuit electronically connected to a fourth address line different from the third address line; a first address decoder electronically connected to the first group of display circuits which selects one or more display circuits from the first group of display circuits; and a second address decoder electronically connected to the second group of display circuits which selects one or more display circuits from the second group of display circuits.

Summary of Invention Paragraph:
[0056] According to this embodiment, the first or second address line may be the same address line as the third or fourth address line. Also according to this embodiment, the first address line and the second address line may be fabricated in poly-silicon. Also according this embodiment, a set of data lines may be connected to two or more display circuits of the plurality of display circuits.

Summary of Invention Paragraph:

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[0057] A method is also provided for reducing a number of address lines in a display matrix. According to one embodiment of the method, the display matrix is constructed so that display circuits are arranged in rows. Local address decoders are positioned in the display matrix so that each local decoder is connected to a plurality of rows of display circuits, wherein the local address decoder selects individual rows from the plurality of rows. Address lines are formed such that each of the local decoders is in electronic communication with an address line.

Summary of Invention Paragraph:
[0059] In another embodiment, a display matrix is provided comprising a plurality of display elements, each display element including a pixel; and a display circuit electrically connected to the pixel, the display circuit including a plurality of memory cells; and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time; wherein at least one component of the selector and at least one component of the memory cells are fabricated using a same fabrication tool.

Summary of Invention Paragraph:
[0060] In another embodiment, a display matrix is provided which comprises a plurality of display elements, each display element including a pixel, and a display circuit including a plurality of memory cells electrically connected to the pixel; and a plurality of strobe lines which control communication between display circuits and the plurality of pixels; wherein at least a portion of the plurality of strobe lines are operatively connected to at least two display elements.

Summary of Invention Paragraph:
[0061] According to this embodiment, the display circuit may optionally further include a selector which controls communication between the plurality of memory cells and the pixel. The selector may comprise a plurality of switches connected to the plurality of memory cells. The selector may be controlled by the portion of the plurality of strobe lines.

Brief Description of Drawings Paragraph:
[0062] FIG. 1 illustrates a display matrix.

Brief Description of Drawings Paragraph:
[0063] FIG. 2 illustrates a display circuit which may be used in the display matrix of the present invention.

Brief Description of Drawings Paragraph:
[0064] FIG. 3 illustrates a prior art display circuit.

Brief Description of Drawings Paragraph:
[0067] FIG. 5 illustrates a backplane integrated circuit (backplane IC) which may be used in a display matrix of the present invention.

Brief Description of Drawings Paragraph:
[0068] FIG. 6 illustrates a configuration of strobe lines connected to display circuits.

Brief Description of Drawings Paragraph:
[0069] FIGS. 7A-7C illustrate three examples of a virtual image display which include a display matrix according to the present invention, and one or more magnification optics.

Brief Description of Drawings Paragraph:
[0070] FIG. 7A illustrates a virtual image display system which includes a display matrix which projects an image onto a back surface of the first magnification optic which reflects (at least partially by total internal reflection) the image to a

surface having a magnification function and a reflection function.

Brief Description of Drawings Paragraph:
[0071] FIG. 7B illustrates a virtual image display system which includes an illumination source which reflects light off the microdisplay system to a beamsplitter which reflects an image formed by the microdisplay to a surface of the first magnification optic having a magnification function and a reflection function.

Brief Description of Drawings Paragraph:
[0072] FIG. 7C illustrates a virtual image display system which includes an illumination source which reflects light off the microdisplay system to a back surface of a first magnification optic which reflects the light to a beamsplitter which reflects the light to a surface of the first magnification optic having a magnification function and a reflection function.

Brief Description of Drawings Paragraph:
[0073] FIG. 8A illustrates the data transfer and display sequence of a prior art display matrix which employs a single memory cell per pixel.

Brief Description of Drawings Paragraph:
[0074] FIGS. 8B and 8C illustrate data transfer and display sequences that may be used when a display matrix according to the present invention which employs two or more memory cells per pixel is operated in an FSC mode.

Brief Description of Drawings Paragraph:
[0075] FIG. 8B illustrates that it is possible to display multiple sub-images of a frame, optionally all the sub-images of a frame, without having to transfer any data into memory.

Brief Description of Drawings Paragraph:
[0076] FIG. 8C illustrates that it is possible to display one sub-image while transferring data for another sub-image into memory.

Brief Description of Drawings Paragraph:
[0079] FIG. 10 illustrates a pair of display circuits and a pair of pixels, wherein the display circuits are partially within the footprints of each of the pixels, and the pixels are partially within the footprints of each of the display circuits.

Brief Description of Drawings Paragraph:
[0080] FIG. 11 illustrates a matrix of display circuits and pixels, wherein multiple data circuits overlap the footprints of multiple pixels, and data lines are connected to multiple display circuits.

Brief Description of Drawings Paragraph:
[0081] FIG. 12 illustrates five display circuits, each of which is partially within the footprint of each of five pixels, wherein a single set of data lines is connected to all five data circuits.

Detail Description Paragraph:
[0089] The present invention relates to a display matrix for forming sequentially formed composite images. As used herein, a sequentially formed composite image is an image formed by displaying a series of two or more different sub-images to an observer where the different sub-images are displayed one sub-image at a time on the display matrix. These display matrices can be used in a display system component of a variety of electronic devices. Examples of such devices include, but are not limited to portable computers, personal communicators, personal digital assistants, modems. pagers, video and camera viewfinders, mobile phones, and television monitors. In one particular embodiment, the display matrices and display systems of the present invention are used in combination with one or more

magnification optics to form a virtual image display system.

Detail Description Paragraph:
[0090] A unique property of the display matrix of the present invention is that data for a plurality of sub-images may be stored in the display matrix simultaneously. This property eases the instantaneous bandwidth requirements of the display matrix and, in certain situations, actually decreases the amount of data which must be transferred to the display matrix from external memory locations.

Detail Description Paragraph:
[0091] In general, a display system forms a sequentially formed composite image by displaying a series of sub-images to an observer at a rate preferably faster than the eye of the observer can resolve. Image quality is reduced if the eye is able to perceive an individual field sub-image, a phenomena known as flicker. In practice, it has been found that frame rates in excess of 60 Hz are necessary to avoid flicker.

Detail Description Paragraph:
[0092] Ideally, the data for any sub-image should be present in the display matrix from the beginning until the end of the display of the sub-image. If the display matrix houses only a single sub-image at a time, then ideally the entire data transfer should take place between the display of one sub-image and the next. This places high instantaneous bandwidth requirements on the system in order to transfer all of the data for a sub-image in the interval between the display of sub-images.

Detail Description Paragraph:
[0093] FIG. 1 illustrates a typical display matrix 12 which includes a plurality of display elements 14. Each display element 14 includes a pixel 16 and a display circuit 18 which is electrically connected to the pixel and controls the operation of the pixel 16. The plurality of pixels incorporated into the plurality of display elements together form the source object formed by the display matrix 12.

Detail Description Paragraph:
[0094] In a display matrix according to the present invention, the display circuit consists of a plurality of memory cells and a selector. The selector is able to output to the pixel the contents of at most one memory cell at any instant. The selector is controlled by additional input signals provided to the display circuit.

Detail Description Paragraph:
[0095] FIG. 2 illustrates a display circuit 18 which may be used in the display matrix of the present invention. As illustrated, the display circuit 18 includes a plurality of memory cells 20A, 20B (two shown) which are each electrically connected to a selector 22. The selector controls which memory cell is electrically connected to the pixel 16. As illustrated, the display circuit 18 can also optionally receive one or more inputs 24 for controlling the operation of the selector 22.

Detail Description Paragraph:
[0096] As illustrated in FIG. 2, a feature of the display circuit and display matrix of the present invention is that a plurality of the memory cells in the display circuit are continuously electrically connected to the selector of the display circuit at the same time. As a result, there is no need to address a particular memory cell to a particular selector. This may be accomplished, as illustrated in FIG. 2, by the display circuit including separate conductive elements 21 for each memory cell in the display matrix which electrically connects a memory cell to the selector in the display circuit. The figure illustrates that all the memory cells in the display circuit are connected. It is noted that less than all of the memory cells may optionally be continuously electrically connected.

Detail Description Paragraph:
[0097] A further feature of the display circuit and display matrix of the present invention is that the display matrix is formed on a substrate having a plurality of regions where each region includes a memory circuit with a plurality of memory cells, and a selector electrically connected to each memory cell in the region. For example, FIG. 1 illustrates a plurality of display circuits in separate regions. By having a plurality of regions which each include a complete memory circuit, a display matrix is provided where the memory cells are physically interdispersed among the selectors within the display matrix. This distinguishes the display matrix of the present invention over prior art displays with an external frame buffer. The substrate may be any material on which the display circuit may be attached or formed. In a preferred embodiment, the substrate is a semiconductor, such as silicon, on which the display circuits are formed by one or more of a variety of methods known in the art.

Detail Description Paragraph:
[0098] Yet a further feature of the display matrix of the present is its ability to store more than one image at a time. Because the display circuit 18 has more than one memory cell per pixel, it is possible to display two or more different sub-images without having to write to the memory cells between displaying the different sub-images. In addition, data may be transferred to the display matrix for one sub-image while a different sub-image is displayed. Accordingly, the data transfer time for one sub-image can be spread over the entire display time of a different sub-image. This alleviates the need for a high instantaneous bandwidth or a high sub-image display rate, a clear advantage over prior art display systems.

Detail Description Paragraph:
[0099] FIG. 3 illustrates a prior art display circuit. As illustrated in FIG. 3, the prior art display circuit includes a single memory cell 20C which is connected to pixel 16. The prior art display circuit thus does not need a selector or input for controlling the operation of the selector. Further, because the display circuit only includes one memory cell 20C, a memory matrix employing this display circuit can only store data for one sub-image and thus cannot display different sub-images without having to write to the memory cells between displaying the different sub-images. When it is necessary to create an image out of a composite of sub-images, the sub-images are typically composed in a spatial relationship and written simultaneously to the matrix.

Detail Description Paragraph:
[0100] The display matrix of the present invention may be any addressable display which includes a pixel and a display circuit which controls the operation of the pixel in response to control signals. As used herein, a pixel (a contraction of picture element) refers to any mechanism which can either emit light or modulate incident light in response to an electrical field to form one element of a source object. The plurality of pixels incorporated into the plurality of display elements together form the source object formed by the display matrix.

Detail Description Paragraph:
[0102] In one embodiment of the present invention, the pixels used in the display matrix are sized to be a microdisplay. As used herein, a microdisplay refers to a display matrix which is used in a virtual image display system to form a source object which is then magnified by one or more magnification optics to form a magnified virtual image. In a preferred embodiment, the microdisplay forms a source object having an area equal to or less than about 400 mm.sup.2. In one embodiment, the source object has an area between about 10 mm.sup.2 and 400 mm.sup.2, more preferably between about 20 mm.sup.2 and 100 mm.sup.2. The pixels of the display matrix preferably have an area less than about 0.01 mm.sup.2 and more preferably between 50 .mu.m.sup.2 and 500 .mu.m.sup.2.

Detail Description Paragraph:
[0103] By designing a microdisplay to include a display circuit according to the present invention, microdisplays with reduced instantaneous bandwidth requirements and reduced average bandwidth are provided. The reduced bandwidth requirements translate into lower power consumption, which is particularly important for battery-powered applications in devices which incorporate microdisplays.

Detail Description Paragraph:
[0104] In one particular embodiment, a microdisplay is provided which includes a liquid crystal device (LCD) and operates in either reflective or scattering modes. FIG. 4A illustrates a cross-sectional view of a liquid crystal device while FIG. 4B illustrates a top-down view of a liquid crystal device. As illustrated in FIGS. 4A and 4B, the LCD 32 is composed of a substrate 34 having a plurality of electrodes 36 corresponding to pixels, liquid crystal 38 arranged on the substrate 34, and a counter electrode 40 arranged on the liquid crystal 38. The liquid crystal is caused to align or relax at each pixel in response to local electric fields applied across the liquid crystal between the pixel and the counter electrode. The potential at each pixel on the substrate is determined by the corresponding display circuit, the design of which is the subject of the present invention. Sequentially changing the potentials at any or all of the pixels on the substrate via the corresponding display circuits causes the LCD as a whole to form a composite image when properly illuminated.

Detail Description Paragraph:
[0106] FIG. 5 illustrates a backplane integrated circuit (backplane IC) which may be used in a display matrix such as a LCD microdisplay. As illustrated, the backplane IC 42 integrates into a single electronic circuit a display matrix 44, programmable registers 46 that generate the control signal logic 48 provided to the display matrix 44 and other timing functions, and an interface 50 to a source of image data. A display matrix for this backplane IC may be sized to include an 800 by 600 two-dimensional array of display circuits.

Detail Description Paragraph:
[0107] The display circuit for a backplane IC according to the present invention is composed of two or more memory cells and a selector circuit. The memory cells may be conventional Static Random Access Memory (SRAM) cells composed of six transistors each, though the use of other digital memory cells is intended to fall within the scope of the present invention.

Detail Description Paragraph:
[0109] As an example of a display circuit, in a three color system, the SRAM cells may be called RED CELL, GREEN CELL, and BLUE CELL, respectively. The cells are addressed for reading and writing via WORD signals. Data is transferred into and out of the SRAM cells via BIT and BIT BAR signals.

Detail Description Paragraph:
[0111] The selector is accomplished with switches that connect the SRAM cells to the pixel at the output of the display circuit. The switches may be pass gates controlled by RED STROBE, GREEN STROBE, and BLUE STROBE signals, respectively. When the RED STROBE signal is asserted, the voltage stored in the RED CELL is transferred to the pixel. The GREEN STROBE and BLUE STROBE signals operate analogously. The various WORD and STROBE signals are provided to each display circuit based on programmable registers inside the backplane IC but outside the display matrix.

Detail Description Paragraph:
[0112] When the RED STROBE is asserted over the entire display matrix, a voltage pattern corresponding to the data stored in the RED CELL of every display circuit is output on the pixels. The GREEN STROBE and BLUE STROBE signals operate analogously.

Detail Description Paragraph:
[0113] In an embodiment of the present invention, each cell is connected to a individual strobe line. This design allows each cell to be strobed individually, thereby minimizing the power consumed in the operation of the display system and optimizing the operation speed of the display.

Detail Description Paragraph:
[0114] In an alternative embodiment, multiple cells are connected to individual strobe lines. This design reduces the wiring density of the IC. By varying the number of strobe lines used, the display system can be designed to have a desired level of wiring density. It is noted that power efficiency and operation speed decrease as wiring density decreases. The particular wiring density that is preferred will depend upon the particular application for which the display is being designed and the wiring density, power efficiency, and operation speed that are required.

Detail Description Paragraph:
[0115] FIG. 6 illustrates an embodiment where the total number of strobe lines in the display system is reduced from a 1:1 strobe line to memory cell ratio by increasing the number of memory cells connected to individual strobe lines. In particular, FIG. 6 illustrates an embodiment where each strobe line corresponding to a color and is connected to a plurality of cells of the respective color so that each STROBE signal controls a plurality of cells of the respective color. The figure depicts four display circuits 600, 602, 604, 606 with three SRAM cells per display circuit. Each display circuit 600 has a RED CELL 608, a GREEN CELL 610, and a BLUE CELL 612. The four RED CELLS (608A-D) are connected to a single RED STROBE 614 by connection 614A the four GREEN CELLS (610A-D) are connected to one GREEN STROBE 616 by connection 616A, and the four BLUE CELLS (612A-D) are connected to one BLUE STROBE 618 by connection 618A. When the RED STROBE signal is activated, the voltages stored in the four RED CELLS connected to the RED STROBE are transferred to their respective pixels. The GREEN STROBE and BLUE STROBE signals operate analogously.

Detail Description Paragraph:
[0116] As can be seen from FIG. 6, it is possible to reduce the number of strobe lines in a display system from a 1:1 strobe line to memory cell ratio by having multiple memory cells be controlled by a single strobe line. It should be understood that depending on the application, it may be desirable to increase the number of strobe lines in order to minimize power consumption at the expense of display thickness or decrease the number of strobe lines in order to reduce the thickness of the display at the expense of power consumption.

Detail Description Paragraph:
[0117] The display matrix of the present invention can be designed to be employed in a wide variety of electronic devices in which a real or virtual image needs to be displayed. In particular, the display matrix is intended for use in small sized electronic devices such as portable computers, personal communicators, personal digital assistants, modems, pagers, video and camera viewfinders, mobile phones, television monitors and other hand held devices.

Detail Description Paragraph:
[0118] In one particular embodiment, the display matrix is employed in a virtual image display system where the display matrix forms a source object which is then magnified by one or more magnification optics. In this embodiment, the display matrix is preferably sized to be a microdisplay.

Detail Description Paragraph:
[0119] FIGS. 7A-7C illustrate three examples of a virtual image display which include a display matrix according to the present invention, and one or more

magnification optics.

Detail Description Paragraph:
[0120] FIG. 7A illustrates a virtual image display system which includes a display matrix 62 which projects an image onto a back surface 63 of the first magnification optic 64 which reflects (at least partially by total internal reflection) the image to a surface 65 having a magnification function and a reflection function. The surface 65 reflects the image to a second magnification optic 66 and to an observer 67.

Detail Description Paragraph:
[0121] FIG. 7B illustrates a virtual image display system which includes an illumination source 69 reflects light off the microdisplay system 62 to a beamsplitter 71 which reflects an image formed by the microdisplay to a surface 73 of the first magnification optic 64 having a magnification function and a reflection function. The surface 73 reflects the image through the beamsplitter 71 to a second magnification optic 66 and to an observer 67.

Detail Description Paragraph:
[0122] FIG. 7C illustrates a virtual image display system which includes an illumination source 75 which reflects light off the microdisplay system 62 to a back surface 77 of a first magnification optic 64 which reflects the light to a beamsplitter 79 which reflects the light to a surface 81 of the first magnification optic 64 having a magnification function and a reflection function. The surface 81 reflects the light through the beamsplitter 79 to a second magnification optic 66 and to an observer 67. Examples of virtual image display systems which can be used include but are not limited to the virtual image display systems described in U.S. Pat. Nos. 5,625,372; 5,644,323; and 5,684,497 which are each incorporated herein in their entirety by reference.

Detail Description Paragraph:
[0123] One feature of the present invention is the efficiency with which the display matrices of the present invention may be operated in a field sequential color (FSC) mode. In a typical FSC mode, a composite image is formed through the repetition of a sequence of different color sub-images, typically red, green, and blue sub-images. As illustrated in FIGS. 8A and 8B, the one or more sub-images 26 corresponding to a color is called a field 28. A single sequence of the different fields is called a frame 29.

Detail Description Paragraph:
[0125] Data transfer requirements for an FSC mode are more stringent than for a general system for sequentially formed composite images. The total length of time that a sub-image may be displayed, from the end of the display of the prior sub-image to the end of the display of the current sub-image, is limited by the minimum frame rate necessary to avoid flicker. The data for a particular sub-image must also be present in the display matrix from the beginning to the end of the sub-image. The quality of the image produced is reduced if part of the one color frame is displayed while a part of another color frame is displayed.

Detail Description Paragraph:
[0126] FIG. 8A illustrates the data transfer and display sequence of a prior art display matrix which employs a single memory cell per pixel. As illustrated, the entire data transfer for a sub-image takes place during a time period T.sub.DT after the time period for displaying the prior sub-image T.sub.DI-1 and before the time period for displaying the current sub-image, also T.sub.DI-2. In order to avoid flicker, the period of time available for data transfer and display is limited by the minimum frame rate T.sub.MFR. The need to transfer the entire data for a sub-image during the time period T.sub.DT which is less than the minimum frame rate T.sub.MFR time period creates a high instantaneous bandwidth requirement on a prior art display matrix operating in an FSC mode. The average bandwidth

requirement, which is a direct function of the frame rate as well, is accordingly high.

Detail Description Paragraph:
[0127] FIGS. 8B and 8C illustrate data transfer and display sequences that may be used when a display matrix according to the present invention which employs two or more memory cells per pixel is operated in an FSC mode. When a display matrix employs two or more memory cells per pixel, it is possible to store data for more than one sub-image, whether of the same or a different field. In one embodiment, the display matrix includes sufficient data to store all of the individual sub-images of a field or the entire composite image simultaneously.

Detail Description Paragraph:
[0128] As illustrated in FIG. 8B, by having sufficient memory to store multiple sub-images, it is possible to display multiple sub-images of a field, optionally all the sub-images of a field, without having to transfer any data into memory. Alternatively, as illustrated in FIG. 8C, by having sufficient memory to store multiple sub-images, it is possible to display one sub-image while transferring data for another sub-image into memory. As discussed herein, the ability to display one sub-image while transferring data for another sub-image into memory enables one to produce more colors and other visual effects than would otherwise be possible due to the greater instantaneous bandwidth requirement of prior art display matrices operated in an FSC mode.

Detail Description Paragraph:
[0129] As demonstrated by the data transfer and display sequences illustrated in FIGS. 8B and 8C, the use of two or more memory cells per pixel in a display matrix significantly reduces the instantaneous bandwidth requirement of the system. In addition, in the case where the data for one particular field sub-image is the same as the that for the next sub-image of the same field, the data for the next sub-image does not need to be transferred at all, reducing the average bandwidth requirement.

Detail Description Paragraph:
[0130] The present invention is intended to encompass display matrices where each memory cell consists of one bit or more than one bit of memory. As used herein, a digital display system refers to a display system where a single binary bit of memory is associated with each memory cell. In this system, the selector outputs a binary value as a function of the data stored in the memory cells, and binary control signals are provided to each display circuit. By binary is meant a two-level voltage system, where each voltage can be represented by either a `0` or a `1`.

Detail Description Paragraph:
[0131] In a digital display system, gray levels within a particular color field may be attained by multiplexing different sub-images of that field. By showing certain sub-images of a field longer than other sub-images, certain sub-images are rendered more significant to the composite field image than other sub-images. For instance, in a display matrix with two memory cells per display circuit, the first memory cell in each display circuit may correspond to the most significant bit (MSB) of the binary representation of the grayscale values for a particular field. The second memory cell in each display circuit may correspond to the least significant bit (LSB). In a display matrix with three memory cells per display circuit, the first memory cell may be the most significant bit (MSB), the second memory cell the second significant bit (SSB), and the third memory cell the least significant bit (LSB).

Detail Description Paragraph:
[0132] By displaying each bit for different portions of the time that a particular frame is displayed, a multiple grayscale field may be formed. One bit may be

displayed for a larger portion of the time that a particular frame is displayed either by displaying that bit longer, as illustrated in FIG. 9A, or by displaying that bit more frequently, as illustrated in FIG. 9B. For example, a four-level grayscale system is achieved in a two bit system when the MSB sub-image is displayed for twice as long as the LSB sub-image. The total display time for both sub-images equals the display time for the field.

Detail Description Paragraph:
[0135] In one embodiment of the present invention, two memory cells are present in each display circuit. Once data has been loaded into the display matrix, it is possible to form either a dichromic composite static image or a four-level grayscale monochromic composite static image. In the dichromic case, one memory cell of each display circuit contains the data corresponding to one color field and to the location of the display circuit within the image. The second memory cell contains the corresponding data for the second field. By cycling between the two sub-images corresponding to the memory cells within each display element, a dichromic composite static image is formed.

Detail Description Paragraph:
[0136] In the four-level grayscale case, the memory cells of each display circuit contain the MSB and LSB of the image data associated with a single color field. By cycling between the two corresponding sub-images, while keeping the total duration of the MSB image twice that of the LSB image, four levels of grayscale are achievable.

Detail Description Paragraph:
[0137] It is noted that in both the dichromic and four-level grayscale cases, if the image is static, there is no need to load data into memory more than once. A display system of the present invention just continues cycling between the two sub-images to achieve the intended effect. Data is only reloaded when the image content changes. In contrast, in a prior art display system with only a single binary memory element in each display circuit, data would have to be loaded in with every sub-image, for both the dichromic and four-level grayscale cases, regardless of whether the image content had changed. Even if the sole memory element were analog, data would still have to be loaded in with every sub-image for the dichromic case.

Detail Description Paragraph:
[0138] In analogy with the two cell case, with three memory cells present in the display circuit, a three-color composite image and an eight-level grayscale monochromic composite image are possible with data reloading not necessary until the image content changes. With four memory cells, three basic cases are possible: (1) a four-color composite image; (2) a dichromic composite image with four levels of grayscale in each color; and (3) a 16-level grayscale monochromic composite image.

Detail Description Paragraph:
[0139] In analyzing display circuits with more than four memory cells, many permutations of numbers of color fields and grayscale levels are possible and are all intended to fall within the scope of the present invention. If the analysis is confined to typical display systems operating in an FSC mode with three fields, some of the interesting display circuits are those with (1) six memory cells for four levels of grayscale per field; (2) nine memory cells for eight levels of grayscale per field; (3) twelve memory cells for 16 levels of grayscale per field; and (4) eighteen memory cells for 64 levels of grayscale per field.

Detail Description Paragraph:
[0140] In general, each memory cell in a display circuit of the present invention corresponds to a sub-image. The sub-images corresponding to different memory cells are output from the display matrix according to the control signals provided to each display circuit. The sub-images can have any order and may be displayed for

any amount of time. For example, a particular sub-image may be displayed more frequently than other sub-images, as in the case of the MSB sub-image. The sub-image may also be displayed for a longer period of time than other sub-images.

Detail Description Paragraph:
[0141] The assignment of, sub-images to different memory cells may be dynamic. In a system with three bits of memory for display element, the assignment of the first, second, and third memory cells as the MSB, SSB, or LSB can be changed, field to field and/or frame to frame. For example, the first memory cell of every display element may at one time be assigned to the MSB sub-image of the red field and at another time to the LSB sub-image of the green field.

Detail Description Paragraph:
[0142] In display systems for sequentially formed composite images, the display image data is transferred to the display matrix from a frame buffer. The frame buffer is typically external to the display system in the sense that the frame buffer is a separate component from the display matrix.

Detail Description Paragraph:
[0143] The purpose of an external frame buffer is to house an entire frame of data and act as an intermediary between some sort of processor, which initializes and modifies the image in the frame buffer, and the display matrix, which displays the image or part thereof. The data transfer bandwidth between the processor and the frame buffer varies according to the rate of change in the content of the image. For example, a static, monochromic image requires essentially zero bandwidth. In a display system operating in an FSC mode with a high frame rate, the bandwidth requirement remains high regardless of how static the image may be.

Detail Description Paragraph:
[0144] A display matrix of the present invention can also be used to store multiple sub-images, for example all the sub-images of a single color field as opposed to an entire frame. For example, with three memory cells in each display element, the memory cells can be assigned to the MSB, SSB, and LSB sub-images of a color field, for a total number of 2.sup.3=8 shades of gray. If the memory cells are then reassigned to corresponding sub-images of the next color field during the display of the next color field, then 8 levels of grayscale will be possible for the next color field as well. For an entire frame, a total of 8.sup.3=512 colors are possible.

Detail Description Paragraph:
[0145] Using a display matrix of the present invention operated in an FSC mode, it is possible to house an entire frame of data in the display matrix itself. For example, a three color FSC system may be built from a display matrix having three memory cells in each display element. Each memory cell would be dedicated to a different color field sub-image. Since there would only be one bit per field, the total number of colors possible in the system would be 2.sup.3=8. With six memory cells in each display element, 4.sup.3=64 colors would be possible.

Detail Description Paragraph:
[0146] The advantage of housing an entire frame of data within the display matrix is that the external frame buffer may be completely eliminated from the display system, saving not only a component but also a great deal of bandwidth. Only the bandwidth between the processor and the display matrix would remain. In contrast, operating a prior art display matrix in FSC mode, there is no room within the display matrix to house multiple sub-images simultaneously, necessitating an external frame buffer.

Detail Description Paragraph:
[0147] One condition for eliminating the external frame buffer is that the display matrix behave like an external frame buffer from the processor point of view. In

particular, the display matrix should behave like a memory: random access addressable as well as readable and writable. In contrast, the display matrix of prior art typically is not random access addressable and is only writable.

Detail Description Paragraph:
[0148] The primary interface to the display matrix from the source of image data can mimic that of a synchronous SRAM. For example, the clocked interface includes a general backplane IC chip select and a read/write signal. An internal write buffer supports consecutive writes to the memory cells in the display matrix and to programmable registers outside the display matrix. The latency to the first read data from either the memory cells or the programmable registers is a fixed number of cycles. Data on consecutive cycles is returned on burst reads. The length of burst accesses can be programmed to be 1, 2, 4, or 8 words, where the length of a word is defined as the data bus width. The latter is initialized to 8 bits on reset, but can be reprogrammed to 8, 16, or 32 bits. A total of 20 address lines can be used to specify the destination of a read or write to the memory matrix.

Detail Description Paragraph:
[0149] A secondary interface optimized for minimum pin count is also possible. The secondary interface can include a vertical synchronization signal, a horizontal synchronization signal, a data enable signal, and a clock, along with 8, 16, 24, 32, or some other intermediate number of bits of data. The secondary interface can be used to scan data into the display matrix only, with no capability to read data from the matrix.

Detail Description Paragraph:
[0150] A variety of actual sources of image data outside the display matrix may be used. For instance, read only memory (ROM), programmable memory such as a field programmable gate array (FPGA), an external frame buffer, or a processor are possible.

Detail Description Paragraph:
[0151] Layout Designs for Display Circuits

Detail Description Paragraph:
[0152] An aspect of the present invention relates to layout designs for positioning a plurality of display circuits adjacent pixels of a corresponding display element. For instance, in a display system of the present invention, there are multiple memory elements per pixel. As the number of memory elements per pixel increases, it becomes increasingly difficult to position the display circuit including the plurality of memory elements adjacent the pixel. It is thus necessary to design the layout of the display matrix to accomodate for display circuits which do not fit within the spatial confine, or "footprint", of the corresponding pixel.

Detail Description Paragraph:
[0153] One aspect of the present invention relates to a display matrix layout design where the display circuit is at least partially positioned outside of the footprint of the pixel. Another aspect of the present invention relates to a display matrix layout design where a display circuit is positioned within the footprint of two or more pixels. Yet another aspect of the present invention relates to a display matrix layout design where two or more display circuits are positioned within the footprint of a pixel. These layout designs allow multiple memory cells to be positioned more closely adjacent each pixel.

Detail Description Paragraph:
[0154] The layout designs described above are illustrated in FIGS. 10-12. FIG. 10 illustrates two rectangular display circuits 202A, 202B placed under two pixels 204A, 204B. Each display circuit is at least partially located within the footprints of both pixels. Additionally, each pixel is placed within the footprints of both display circuits. However, each of the display circuits has an electrical

connection to only one of the pixels 206A, 206B, thereby preserving the correspondence of one pixel to one display circuit in each display element.

Detail Description Paragraph:
[0155] One feature of the layout designs illustrated in FIGS. 10-12 is the positioning of multiple address lines under each pixel or under each row of pixels. In order to facilitate random access to the memory elements of each display circuit, each of the display circuits must be separately addressable. This requires each display circuit to be connected to an address line. When two or more display circuits are placed in the footprint of a pixel, the same number of address lines are placed under the pixel, one for each display circuit.

Detail Description Paragraph:
[0156] The positioning of multiple address lines under each pixel and under a row of pixels is illustrated in FIG. 10. Each of the display circuits 202A and 202B is connected to a single address line, 208A and 208B, respectively. But since both display circuits lie within the footprint of one pixel 204A, there are two address lines running under one row of pixels 212 in the display matrix.

Detail Description Paragraph:
[0157] The layout illustrated in FIGS. 10-12 were multiple display circuits are positioned within the footprint of a pixel provides a further advantage of enabling a substantial decrease in the number of data lines (e.g., bit and bit bar lines) used in the display system. By placing multiple display circuits within the footprint of an individual pixel, multiple data circuits can be connected to a single pair of bit and bit bar lines. The layout also results in an increase in the number of address lines that are used in the display system in order to preserve random access to the memory elements in the display system. However, the reduction in the number of data lines is more significant.

Detail Description Paragraph:
[0158] Each display circuit in the display matrix connects to a BIT line and a BIT BAR line. By placing multiple display circuits within the footprint of each pixel, each display circuit within the footprint of a pixel can be connected to the same BIT and BIT BAR lines. This allows for a net reduction in the number of BIT and BIT BAR lines connected entering the display system.

Detail Description Paragraph:
[0159] How the number of data lines can be reduced according to the present invention will now be illustrated with regard to FIGS. 10-12. In FIG. 10, display circuits 208A, 208B are both located under pixel 204A and pixel 204B. An address line is provided for each display circuit, shown in the figure as address lines 208A, 208B. Meanwhile, a single pair of data lines (BIT 210A and BIT BAR 210B) are used for both display circuits. As-a result, only 4 data and address lines are employed. By contrast to FIG. 10, one could use a single address line for both display circuits and two data lines for each display circuit (not shown). This, however, would result in 5 data and address lines being used.

Detail Description Paragraph:
[0160] FIG. 11 illustrates another embodiment where there are two rows and four columns of pixels (300A, 300B, 300C, 300D and 302A, 302B, 302C, 302D). Each row of pixels is divided into two pairs with a pair of display circuits (304A-H) being positioned underneath the pair of pixels, as in FIG. 10. Two address lines (306A-D) are positioned under each row of pixels and a pair of data lines (308A-D) are provided for each two columns of pixels. As illustrated in FIG. 11, a total of 8 data and address fines are employed. By contrast, if BIT and BIT BAR lines were used for each column of pixels, and an address line were used for each row of pixels, 10 data and address lines would be employed.

Detail Description Paragraph:

h e b b g e e e f c e f e ge

[0161] FIG. 12 illustrates yet another embodiment where there are five display circuits (402A-E) and five address lines (404A-E) running under the display circuits. Meanwhile, a single set of data lines (406A-B) are used for the five display circuits. As can be seen, only 7 data and address lines are used. By contrast, if one were to use 1 address line and 5 pairs of data lines per row of pixels, a total of 11 data and address lines would be used. As can be seen from FIG. 12, the reduction in the number of data lines becomes more significant as the number of memory cells per display circuit increases.

Detail Description Paragraph:
[0162] The layout designs illustrated in FIGS. 10-12 provide a substantial reduction in the number of lines used in the display matrix. For example, suppose a display matrix consists of 600 rows and 800 columns of pixels where each display circuit includes 3 memory cells. Assume each display circuit is positioned within the footprint of each pixel. This results in a corresponding matrix of display circuits which are arranged into 600 rows and 800 columns. Each row of display circuits in such a layout would be connected to an address line, thus requiring 600 address lines. Each column of display circuit would be connected to 3 pairs of data lines, one pair per memory cell. Since there are 800 columns, there would need to be 4800 data lines. Combined, a total of 5400 lines are needed.

Detail Description Paragraph:
[0163] Now lets assume one lays out a display matrix consisting of 600 rows and 800 columns of pixels as illustrated in FIG. 11. Each row is connected to two address lines. For 600 rows there would be 1200 address lines. Meanwhile, only three pairs of data lines are used for every two columns. For 800 columns there would be 2400 data lines. Combined, a total of 3600 lines are needed.

Detail Description Paragraph:
[0164] In another example, suppose a display matrix consists of 600 rows and 800 columns of pixels where each display circuit includes 5 memory cells. Assume each display circuit is positioned within the footprint of each pixel. According to this layout design, there would be 600 address lines (1 address line per row) and 8000 data lines (800 columns.times.2 lines per memory cell.times.5 memory cells) for a total of 8600 lines.

Detail Description Paragraph:
[0165] Now lets assume that one lays out a display matrix consisting of 600 rows and 800 columns of pixels as illustrated in FIG. 12. Each row is connected to five address lines so 600 rows would require 3000 address lines. Meanwhile, only five pairs of data lines are used for every five columns. For 800 columns there would be 1600 data lines (800 columns.times.10 lines per 5 columns). Combined, a total of 4600 lines are needed. As can be seen, the reduction in the number of data lines becomes quite significant as the number of memory cells per display circuit increases.

Detail Description Paragraph:
[0167] An aspect of the present invention relates to the use of local decoding of row addresses in the display system to reduce the number of address lines, or "word lines," in the display system. According to this layout technique, decoders are inserted at periodic intervals in the display matrix. These decoders are connected to surrounding display circuits, so that each decoder is connected to rows of the display matrix. Each decoder receives a word line, two sub-word lines, and an enable line. The sub-word lines supply two bits, a Most Significant Bit (MSB) and a Least Significant Bit (LSB) which provide an offset for selecting one of the rows connected to the decoder. This obviates the need to connect an address line to each of the rows connected to the decoder. The enable bit is used to minimize power consumption.

Detail Description Paragraph:

h e b b g e e e f c e f e ge

[0168] FIG. 13 is a schematic illustration of local decoding. In this example, the local decoder 500 is connected to four rows of display circuits 502A, 502B, 502C, 502D in the display matrix. The rows of display circuits connected to the local decoder 500 are referred to herein as a cluster of display circuits. There are three lines entering the local decoder from above. Two of these are most significant bit MSB 504 and the least significant bit LSB 506, which decode which of the four rows connected to the decoder is being addressed. The third line entering the local decoder from above is an enable bit 504, intended to save power. The data lines serve as sub-address lines by controlling which display circuits are being operated by the local decoder.

Detail Description Paragraph:
[0170] The connection of the rows to the decoder, coupled with the offset provided to the local decoder, can be used to reduce the number of address lines connected to the rows of the display matrix. In particular, the number of address lines may be reduced by a factor equal to the number of values that can be denoted by the offset. To illustrate, consider FIG. 13. As there are four rows connected to the decoder, each of these four rows may be selected by one of the four values of the offset. Thus, to select one of these four rows, the display system needs only one word line connected to the decoder, and a pair of sub-word lines to select one of those four rows connected to the decoder. Thus, the number of address lines used in the display system can be reduced by a factor of four.

Detail Description Paragraph:
[0171] In the example of FIG. 13, the local decoders are placed after every 16 pixel columns. Thus, if there are 800 pixel columns in the display matrix, there are 800/16=50 decoders per row. As there are three lines entering each decoder, i.e., the sub-word lines MSB, LSB, and the enable bit, there are 50.times.3=150 additional lines entering the display matrix. However, if there are 600 rows, the number of address lines are reduced by a factor of four, to 150, resulting in 450 fewer address lines. Thus, the addition of the 150 offset and enable lines is countered by a decrease in 450 address lines.

Detail Description Paragraph:
[0172] The insertion of local decoders also confers benefits during fabrication of the display system, as it obviates the need to fabricate word lines in metal. The present embodiment eliminates the need for global word lines which span each row of display circuits, as global word lines are replaced with relatively short interconnects between decoders. The relative brevity of the interconnects allows them to be fabricated in poly-silicon rather than metal. The absence of metal word lines in the IC results in improved packing density, and frees space for other metal interconnects.

Detail Description Paragraph:
[0174] The display circuit layout designs described above, for example with regard to FIGS. 10-12, can be combined with local decoding to produce a drastic reduction in the number of address and data lines entering the display matrix. As illustrated in regard to FIGS. 10-12, the number of data lines can be significantly reduced by connecting data lines to multiple data circuits. The resulting increase in address lines can then be diminished by replacing global word lines with local decoders.

Detail Description Paragraph:
[0175] The synthesis of these techniques can be illustrated by example. Consider a display matrix which consists of 600 rows by 800 columns and 3 memory elements per pixel. A display system with exactly one data circuit within the footprint of each pixel has 5400 total lines including 600 address lines and 4800 data lines [800.times.3 BIT lines and 800.times.3 BIT BAR lines]. By designing the display circuits so that two display circuits overlap each pixel (as in FIG. 11), the number of address lines is doubled to 1200, but the number of BIT and BIT BAR lines reduced to 2400, for a total of 3600 lines. If we then apply local decoding as

shown in FIG. 13, the number of address lines is reduced by a factor of 4, reducing the number of address lines to 1200/4=300. Hence, by employing the layout and local decoding techniques described above, a grid of 600 address lines and 4800 data lines can be replaced by a grid of 300 address lines and 2400 data lines.

Detail Description Paragraph:
[0176] Modes of Operating the Display Matrix

Detail Description Paragraph:
[0177] Several different modes for operating a display matrix according to the present invention are possible. One mode, referred to herein as the "Power Miser Mode," relates to a mode where writing to the display matrix is minimized, there reducing the amount of energy consumed by the display matrix. Another mode of operation, referred to herein as the "Color Rich Mode," relates to a mode where data is written to memory cells forming one bit plane while memory cells of another bit plane are used to display an image in order increase the number of sub-images that can be used to form a composite image. By being able to increase the number of sub-images that can be used to form a composite image, a greater number of colors may be formed by the display matrix. Yet another mode of operation, referred to herein as the "Color Mixing Mode," involves operating a display matrix in a Power Miser Mode and Color Rich Mode at the same time.

Detail Description Paragraph:
[0178] While the Power Miser, Color Rich, and Color Mixing modes for operating a display matrix according to the present invention are provided below, it is noted that many additional modes of operating the display matrices can be employed.

Detail Description Paragraph:
[0180] One mode of operating a display matrix according to the present invention is illustrated in FIG. 14 in which a processor 54 interfaces directly with the display matrix (backplane IC) 42. This mode is referred to herein as power miser mode because the image is initialized and modified directly in the display matrix memory without the use and associated power consumption of an external frame buffer. Because the backplane IC is fundamentally digital in nature, component and power consumption costs associated with digital-to-analog converters or other analog circuitry is avoided.

Detail Description Paragraph:
[0181] In operation, the backplane IC offers several functions in support of power miser mode. The synchronous SRAM interface on the chip coincides with the memory model assumed by typical processors. By using three memory cells per display circuit, the chip also offers capacity for a red, a green, and a blue bit plane, the minimum necessary for a display matrix to operate in an FSC mode. The chip can also be programmed for FSC control, a sequence such as the following:

Detail Description Paragraph:
[0188] In an eight-level grayscale monochrome implementation of power miser mode, the RED, GREEN, and BLUE cells of each display circuit are filled with the MSB, SSB, and the LSB of the corresponding image data. The three bit planes can be strobed in a variety of time modulation schemes to achieve the eight levels of grayscale in the color of the single illumination source. One possibility is to strobe the bit planes in RMS fashion using distributed binary coding as described later.

Detail Description Paragraph:
[0190] FIG. 15A illustrates an address map including scroll buffers. The address bus illustrated in the figure is 20 bits wide. Bits A.sub.6 through A.sub.0 specify the column address of a byte, A.sub.16 through A.sub.7 its row address, and A.sub.18 through A.sub.17 its bit plane address. This address scheme assumes the three SRAM cells in each display element have been configured for separate address

(WORD) signals. The address space of the display matrix encompasses 0-99 in the column address, 0-599 in the row address, and 0-2 in the bit plane address. Bit A.sub.19 is the programming bit.

Detail Description Paragraph:
[0197] A second embodiment of scrolling is illustrated in FIG. 15B. A scroll region is first defined. In FIG. 15B the region is eight pixels high by eight pixels wide. However, it can be any region within the display matrix on a one-pixel boundary in the vertical direction and a two pixel-boundary in the horizontal direction.

Detail Description Paragraph:
[0199] Scrolling is an example of hardware assistance for a graphical operation that is outside the operation of display matrices of prior art. By subsuming the external frame buffer within the display matrix of the present invention in power miser mode, a wide variety of hardware assistance functions for image modification become possible and useful within the display matrix.

Detail Description Paragraph:
[0201] A second mode of operating a display matrix according to the present invention is illustrated in FIG. 16, in which an external frame buffer 56 is placed between the processor 54 and the display matrix (backplane IC) 42. This mode is referred to herein as color rich mode, because the multiple bit planes in the display matrix are used to generate multiple levels of grayscale in each of the color fields. For example, when three bit planes are used, eight levels of grayscale (2.sup.3) are produced in each of three color fields for a total of 512 colors (8.sup.3) in FSC operation.

Detail Description Paragraph:
[0204] Transfer the MSB, 2.sup.nd SB, and LSB bit planes of the red image into the RED, GREEN, and BLUE memory planes of the display matrix.

Detail Description Paragraph:
[0209] Transfer the MSB, 2.sup.nd SB, and LSB bit planes of the green image into the BLUE, GREEN, and RED planes of the display matrix.

Detail Description Paragraph:
[0214] Transfer the MSB, 2.sup.nd SB, and LSB bit planes of the blue image into the RED, GREEN, and BLUE planes of the display matrix.

Detail Description Paragraph:
[0221] One algorithm that has been found empirically to have a better RMS effect than the above conventional coding scheme for a particular LCD is called distributed binary coding. A better RMS effect refers to the gradation in voltages driven on the liquid crystal being more uniform. The strobing formula for distributed binary coding is {MSB, SSB, MSB, LSB, MSB, SSB, MSB}. For example, 0= {0000000}, 1={0001000}, 2={0100010}, 3={0101010}, 4={1010101},5={1011101}, 6= {1110111}, and 7={1111111}. In FIG. 18, distributed binary coding is used to display a grayscale 3 in the red field followed by a 6 in the green field.

Detail Description Paragraph:
[0222] While the above formula relates to the present invention with three bit planes, distributed binary coding can be extended to display matrices of any number N of bit planes. The interval is first always divided into (2.sup.N-1) time slots. The MSB plane time slots are determined first. The MSB plane is always placed in the first time slot and every other time slot there after. The 2.sup.nd SB plane time slots is calculated next. The SSB plane is placed in the first available time slot and every fourth time slot thereafter. The 3.sup.rd SB occupies the next available time slot and every eighth slot thereafter, and so on until the LSB (N.sup.th) plane is place in the middle time slot. For instance, for four bit planes, the formula is {MSB, 2.sup.nd SB, MSB, 3.sup.rd SB, MSB, 2.sup.nd SB, LSB,

MSB, 3.sup.rd SB, MSB, 2.sup.nd SB, MSB}.

Detail Description Paragraph:
[0223] The ability of the display system of the present invention to perform distributed binary coding is a strong example of one of the advantages that the display circuit of the present invention provides. The grayscale level is strobed twice in one color field, once in the RECOVERY period and once in the ACTIVE period, for a total of 14 time slots. In a system with only one memory cell per display circuit, fourteen bit planes would have to be loaded in in order to strobe during 14 different time slots. This would require a very high bandwidth transfer rate and pixel refresh rate. However, by using a display matrix capable of storing three different bit planes, different bit planes need not be continuously written into a display matrix. This allows strobing the transition between strobing different bit planes to be significantly reduced, thereby making it possible to have 14 time slots.

Detail Description Paragraph:
[0224] According to the present invention, it is possible to alternate the assignment of MSB memory matrices for consecutive color fields. This enables the display matrix to further take advantage of having more than one memory cell in each display circuit. For instance, in the above sequence, the {RED, GREEN, BLUE} memory matrices were assigned to {MSB, SSB, LSB} for the RED field, while in the ensuing GREEN field, the assignments were switched to {LSB, SSB, MSB}. This algorithm is driven by the nature of distributed binary coding, in which the LSB plane always falls in the middle time slot while the MSB plane is always at the beginning. Once the LSB plane for the ACTIVE period of the RED field has completed, the memory plane can be used for the first plane needed by the GREEN field, which is the MSB plane. Hence, by modifying the assignment of the bit planes as MSB, SSB and LSB, etc., it is possible to increase the number of bit planes which can be written to memory and strobed.

Detail Description Paragraph:
[0225] Distributed binary coding and the accompanying strategies discussed above have been found empirically preferable for certain liquid crystal formulations. Other algorithms may be better suited for other display matrices and are intended to fall within the scope of the present invention.

Detail Description Paragraph:
[0229] A third mode of operating a display matrix according to the present invention, referred to herein as color mixing, relates to the overlay of a color rich region on a power miser background. This mode of operation is illustrated in FIG. 18. By combining color rich operation with power miser operation, a window of high information content can be formed without incurring the bandwidth and power consumption costs associated with full-screen color rich operation. The reduction in bandwidth requirements improves the compatibility of the display matrix with video applications. An example of a color mixing procedure that may be employed is as follows:

CLAIMS:

1. A display matrix comprising: a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel and at least partially positioned outside of a footprint of the pixel, the display circuit including a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time.

2. The display matrix according to claim 1, wherein the plurality of memory cells includes at least 2 memory cells.

3. The display matrix according to claim 1, wherein the plurality of memory cells includes at least 3 memory cells.

4. The display matrix according to claim 1, wherein the plurality of memory cells includes between 2 and 9 memory cells.

5. The display matrix according to claim 1, wherein the plurality of memory cells includes at least 9 memory cells.

6. The display matrix according to claim 1, wherein the memory cells are static random access memory (SRAM) cells.

7. The display matrix according to claim 1, wherein a first display element has a display circuit of second display element at least partially positioned inside the footprint of the pixel of the first display element.

8. The display matrix according to claim 1, further including a data line electronically connected to both a first display circuit of a first display element and a second display circuit of a second display element, the data line enabling reading from and writing to the first and second display circuits.

9. The display matrix according to claim 1, further including two or more data lines, each data line electronically connected to both a first display circuit of a first display element and a second display circuit of a second display element, the data line enabling reading from and writing to the first and second display circuits.

10. The display matrix of claim 9, wherein the two or more data lines comprise a first data line which carries a bit signal, and a second data line which carries a bit bar signal.

11. A display matrix comprising: a first display element including a first pixel, and a first display circuit including a plurality of memory cells electrically connected to the first pixel; a second display element including a second pixel, and a second display circuit including a plurality of memory cells electrically connected to the second pixel, the second display circuit being at least partially positioned within a footprint of the second pixel and within a footprint of the first pixel.

12. The display according to claim 11, wherein the first display circuit is at least partially positioned within the footprint of the second pixel.

13. The display matrix according to claim 12, further including a set of data lines is electronically connected to the first display circuit and the second display circuit, the set of data lines enabling reading to and writing from the first display circuit and the second display circuit.

14. A virtual image display system comprising: a display matrix including a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel and at least partially positioned outside of a footprint of the pixel, the display circuit including a plurality of memory cells, and a selector continuously electrically connected to more than one of the plurality of memory cells, the selector outputting to the pixel data from one memory cell at a time; peripheral control circuits for controlling read and write operations to the memory cells; and one or more magnification optics for magnifying the sub-images formed by the display matrix.

15. The virtual image display system according to claim 14, further including a light emitting mechanism provided at each pixel.

16. The virtual image display system according to claim 14, further including a light modulating mechanism provided at each pixel.

17. The virtual image display system according to claim 16, further including an illumination source for illuminating the pixels.

18. The display system according to claim 16, wherein the light modulating mechanism is a liquid crystal material.

19. A virtual image display system comprising: a display matrix comprising a first display element including a first pixel, and a first display circuit including a plurality of memory cells electrically connected to the first pixel, a second display element including a second pixel, and a second display circuit including a plurality of memory cells electrically connected to the second pixel, the second display circuit being at least partially positioned within a footprint of the second pixel and within a footprint of the first pixel; peripheral control circuits for controlling read and write operations to the memory cells; and one or more magnification optics for magnifying the sub-images formed by the display matrix.

20. The virtual image display system of claim 19, wherein the first pixel is partially within the footprint of the second pixel.

21. The virtual image display system of claim 19, wherein a set of data lines is connected to the first display circuit and the second display circuit, the set of data lines enabling reading to and writing from the first and second display circuits.

22. The virtual image display system according to claim 19, wherein the display system is a display component of a device selected from the group consisting of portable computers, personal communicators, personal digital assistants, modems, pagers, video and camera viewfinders, mobile phones, and television monitors.

23. A method for reducing the number of address lines in a pixel-based display system, the method comprisng: electrically connecting a plurality of display circuits to a plurality of pixels each having a footprint, the plurality of display circuits controlling the operation of the plurality of pixels; positioning the plurality of display circuits relative to the plurality of pixels such that at least a portion of the plurality of display circuits are not entirely positioned within the footprint of a single pixel; and connecting data lines to the plurality of data circuits to read and write data to the plurality of data circuits.

28. The method according to claim 23, wherein positioning the plurality of display circuits includes positioning at least a portion of the plurality of display circuits within the footprint of at least two pixels.

29. The method according to claim 23, wherein positioning the plurality of display circuits includes positioning at least a portion of the plurality of display circuits within the footprint of at least three pixels.

L3: Entry 19 of 33 File: USPT Jan 13, 2004

DOCUMENT-IDENTIFIER: US 6678834 B1
TITLE: Apparatus and method for a personal computer system providing non-distracting video power management

Abstract Text (1):
To change the frequency of a video clock without adversely affecting a display quality. To lower the frequency of a video clock, following steps are executed, detecting an opportunity which causes the reduction of the frequency of the video clock; lowering the frequency of the video clock in a frequency range within which a circuit employing the video clock (for example, a PLL (Phase Lock Loop) circuit) can follow a change in the frequency; and iterating the step of lowering the frequency of the video clock until a predetermined frequency is attained. In addition, the following steps are also performed, detecting an opportunity which causes the reduction of the frequency of the video clock; lowering the frequency of the video clock to a predetermined frequency during a vertical blanking interval of a display device that employs the video clock; and maintaining the predetermined frequency of the video clock until change of the frequency is required. Furthermore, the following steps are performed, detecting an opportunity which causes the reduction of the frequency of the video clock; changing a display color on a screen of a display device to a color for which flickers are not outstanding; and lowering the frequency of the video clock.

Brief Summary Text (2):
The present invention relates to power management, more particularly to a technique for enabling the power management by lowering the frequency of a video clock (Vclk). The Vclk is a timing signal for displaying on a display device, and includes, for example, a timing signal for outputting display data to an LCD (liquid crystal display) for each pixel.

Brief Summary Text (4):
A technique that is currently employed to reduce the power consumed by electronic circuits involves lowering the frequency of a clock, or halting the clock. Since in recent practice there has been an increase in the power consumed by a CPU (central processing unit), the clock frequency is lowered, or halted, in accordance with the amount of processing required for the CPU. The frequency of a video clock, as it is related to a display device such as an LCD, tends to increase with the resolution and the number of display colors, and accordingly, this causes an increase in the power consumption. However, since lowering the frequency of the video clock causes flickers and deterioration of display quality, it is not employed in normal display devices.

Brief Summary Text (5):
Techniques that are employed to lower the frequency of the video clock, or to reduce the refresh rate of the display device are given hereinafter. It should be noted that reducing the refresh rate is not equivalent to lowering the frequency of the Vclk. The refresh rate can be reduced by extending the horizontal or vertical blanking interval while maintaining the Vclk frequency, or by lowering the Vclk frequency, which is the clock frequency on which all the clocks associated with the display are based, without altering the number of clocks used during a horizontal/vertical blanking interval. Lowering the frequency of the Vclk is an

effective means to reduce the power consumption, however, in the present invention, it is used to reduce the refresh rate.

Brief Summary Text (6):
U.S. Pat. No. 5,524,249 discloses a technique for halting. When the supply of power to a display device is halted, a Pclk (substantially the same as a video clock) provides for the lowering the frequency of an Mclk (memory clock: a drive frequency of a video controller) when the supply of the power to a display device is halted in such a suspended state or a standby state. However, there is no description about the manner that the Pclk is lowered or halted during the normal state other than the power saving mode, such as the suspended state or the standby state, and that the Pclk and Mclk are simultaneously lowered in the normal state.

Brief Summary Text (7):
U.S. Pat. No. 5,615,376 discloses a technique for halting a VCLK (video clock) during the horizontal and vertical blanking intervals and for lowering an MCLK when there is no access to the frame buffer. However, no description is given for a technique for lowering the VCLK during a normal display period, and for simultaneously lowering the VCLK and the MCLK in the normal state.

Brief Summary Text (8):
Japanese Unexamined Patent Publication No. Hei 7-64665 discloses a technique for slowing the display timing for an LCD when no data has been written to a display memory for a predetermined period of time and the stored contents have not been changed, if a power voltage drop has been detected, or if the system has fallen into the sleep state. However, no description is given for countermeasures to be taken when flickers occur due to slowing the display timing, and for a technique to be employed to slow the display timing without affecting the display contents.

Brief Summary Text (9):
Japanese Unexamined Patent Publication No. Hei 7-239463 discloses that in an active matrix display device, a refresh operation is performed for several lines (for example, every fourth line in the total of 20 lines) within one frame on the display device, then several frames (four frames, in the above example) are required to refresh the entire screen. In this technique, the above refresh operation is performed as a countermeasure for flickers; however, the effect provided by the operation is inadequate or not satisfactory. In addition, to perform the operation, a circuit provided for a panel must be altered.

Brief Summary Text (10):
Japanese Unexamined Patent Publication No. Hei 6-342148 discloses that in a ferro-electrical liquid crystal display device, only scanning lines in which image data have been altered are refreshed, so that motion picture display such as cursor movement, smooth scrolling, and multi-window, and animated video displays can essentially be performed at high speeds even at the low frame frequency. These operations employ characteristics inherent to the ferro-electrical liquid crystal display device.

Brief Summary Text (11):
Japanese Unexamined Patent Publication No. Hei 9-5789 discloses a technique for lowering the drive frequency of a liquid crystal display device that can rewrite a single pixel arbitrary in the entire pixels. The drive frequency is selected by using a display color, or a motion or a still picture. In addition, it discloses a technique whereby, regardless of whether a still picture or a motion picture is used, the drive frequency is changed in accordance with how much the image to be displayed causes flickers, so that the power consumption is optimized for each display image. The luminance and the display color are also taken into account. However, a special liquid crystal display device that can rewrite a single arbitrary pixel is required.

Brief Summary Text (12):
Japanese Unexamined Patent Publication No. Hei 8-179269 discloses a technique whereby, in order to prevent the occurrence of flicker, data for a positive display having a bright background color and data for a negative display having a dark background color are separately extracted from display data, and the frame frequency of the positive display is raised, while that of the negative display is lowered. However, according to this technique, only two display types, positive and negative, can be identified, and there is no detailed explanation of when the frame frequency should be changed or what method can be used to change it.

Brief Summary Text (14):
Therefore, the problems identified and addressed by the present invention provide for objectives, which include the goals of changing the frequency of a video clock without affecting a display quality. It is yet another objective of the present invention to lower more so the power consumption.

Brief Summary Text (15):
According to a first aspect of the present invention, a method for lowering a frequency of a video clock, includes the steps of detecting an opportunity which causes a reduction of the frequency of the video clock; lowering the frequency of the video clock in a frequency range within which a circuit employing the video clock (a PLL (phase lock loop) circuit in the embodiment) can follow a change in the frequency; and iterating the step of lowering the frequency of the video clock until a predetermined frequency is attained. As a result, a disarrangement of the display contents due to the disruption of the operation of the PLL circuit and etc. can be prevented.

Brief Summary Text (16):
According to another aspect of the present invention, a method for lowering a frequency of a video clock includes, the steps of detecting an opportunity which causes the reduction of the frequency of the video clock; lowering the frequency of the video clock to a predetermined frequency during a vertical blanking interval of a display device that employs the video clock; and maintaining the predetermined frequency of the video clock until change of the frequency is required. Even for a portable computer that employs an LCD display device, the vertical blanking intervals exist just in case the computer is connected to a CRT. Since no display operation is performed during these intervals, by changing the frequency of the video clock during these intervals power saving can be performed without the display contents being disarranged.

Brief Summary Text (17):
According to a third aspect of the present invention, a method for lowering a frequency of a video clock, includes the steps of detecting an opportunity which causes the reduction of the frequency of the video clock; changing a display color on a screen of a display device to a color for which a flicker is not outstanding; and lowering the frequency of the video clock. Conventionally, a technique for changing a drive frequency based on the display color has been disclosed (Japanese Unexamined Patent Publication No. Hei 9-5789), but according to this technique, the frequency of the video clock is never lowered. That is, in the environment provided by Windows 95 (Trademark of Microsoft Corp.) many display colors are employed for which the flicker will become outstanding when the frequency of the video clock is lowered, so that no power will be saved when the method which is based on the display colors is employed. Therefore, to achieve the low power consumption, before lowering the frequency of the video clock, the colors of a display screen are changed to colors for which the flicker is not outstanding. This method is particularly effective for a portable computer when the remaining battery power becomes low while a relatively static application, such as a word processing program, is being executed.

Brief Summary Text (18):

An opportunity which causes the reduction of the frequency of the video clock can be detected in accordance with the type of application whose window is displayed on a screen of a display device. For example, the opportunity is a case where an application is being executed for which the display contents are not frequently changed, and the window of that application is in the foreground and no window is being displayed for another application whose display contents are frequently changed.

Brief Summary Text (19):
The opportunity which causes the reduction of the frequency of the video clock can be a change in the size of a window displayed on the screen of the display device. If, for example, the window of an application whose display contents are frequently changed is minimized, the frequency of the video clock can be lowered.

Brief Summary Text (21):
In addition, the opportunity which causes the reduction of the frequency of the video clock can be a change of the processing contents of a processor. Normally, if the number of commands executed by the processor is reduced, the degree of alteration of the display screen is also reduced. When this change is detected, the frequency of the video clock can be lowered.

Brief Summary Text (22):
A drive frequency of a video controller can be lowered together with the frequency of the video clock. With some disclosed conventional techniques, lowering the frequency of the Mclk occur at the same time as the video clock is halted; however, this never occurs during a normal display operation. In other words, the conventional technique does not teach lowering the drive frequency of the video controller during a normal display period, which is the main feature of the present invention.

Drawing Description Text (9):
FIG. 7 is a timing chart for explaining a front porch and a back porch, with (a) showing a display timing, (b) showing a horizontal synchronization signal and (c) showing a vertical synchronization signal.

Detailed Description Text (8):
If the frequency of the Vclk is to be changed, the frequency can be raised or lowered, and the process differs according to whether it is raised or lowered, see step 130. If a window for displaying motion pictures newly appears on the screen or is moved to the foreground, the frequency of the Vclk must be raised, see step 160. The frequency of the Vclk must be raised as rapidly as possible, or the deterioration of usability such as flickers or disarrangement of display contents occurs.

Detailed Description Text (9):
On the other hand, if the frequency of the Vclk is lowered, even of the frequency of the Vclk is not lowered so immediately, the usability will not be deteriorated. Therefore, by using this, a user is notified of lowering the frequency of the Vclk, see step 140. This is an optional step. This notification may be performed by displaying a pop-up window or by voice. A user may be notified not only that the frequency of the Vclk can be lowered, but also that the frequency can be further lowered by changing display colors so as to further reduce the power consumption. Flickers are caused by lowering the frequency of the Vclk, however, a person is not always sensitive to flickers in any colors of the display. There is a color combination at which a person is not perceptive to flickers. For example, if black and white or colors composed of a combination of the primary colors RGB (red, green and blue) that do not include half tones are used, flickers are rarely sensed by a person. In addition, if a color combination called high contrast (white) which is chosen in the screen design of Windows 95, is used, a user is rarely perceivable of flickers. Therefore, if colors of parts of a displayed window are changed to a

combination of colors at which a user seldom perceive flickers, the frequency of the Vclk can be lowered further. The processing for changing colors is shown in FIG. 2. The change of colors may be performed without notifying a user; however, since a user may mistakenly regard the change as a malfunction, it is preferable that a notification be issued at least one time.

Detailed Description Text (18):
The operation performed by the computer 1 is hereinafter described. The processor 1 transmits data and commands required for drawing via the bus 5 to the video controller 7. The bus interface 13 of the video controller 7 exchanges data with the bus 5 to supply data to be processed to the controller 15. The controller 15 reads from and writes to the frame buffer 29, performs the drawing operation, and controls the video controller 7. In order to periodically refresh the LCD panel 27, the controller 15 also outputs the contents of the frame buffer 29 to the LCD output circuit 17. The LCD output circuit 17 outputs RGB display data at the speed of the Vclk, and also a horizonal synchronization signal Hsync and a vertical synchronization sinal Vsync. For the EMI countermeasure, the LVDS1 (19), which is driven at the speed of the clock supplied by the PLL3 (21), converts RGB digital signals into individual RGB serial differential voltage signals, and transmits them to the LVDS2 (25). Upon receipt of these signals, the LVDS2 (25) outputs the RGB data to the data driver 33 at the speed of the Vclk, and also outputs the Hsync signal and the Vsync signal to the gate driver 31. In this process, the LVDS2 (25) employs a clock signal supplied by the PLL4 (23) to precisely receive the signals from the LVDS1 (19) and to output a signal at the speed of the Vclk.

Detailed Description Text (22):
Since the oscillation of the PLL3 (21) does not become unstable if above operation is performed, no disorderliness is transmitted to the circuits following the LVDS2 (23), display contents are not disarranged, and usability is not deteriorated. The frequency of the PLL is generally specified by three parameters: a numerator, a denominator and a frequency divider. If values near the current parameters are employed as values to be set next, it is possible to suppress instability of the PLL due to a difference in the timings at which individual parameters are loaded to a phase detector of the PLL circuit. Assuming that "numerator=15 and denominator=23" and the refresh rate is 60 Hz, it is preferable that, to change to a refresh rate of 59 Hz, "numerator=15 and denominator=22" be set as near-by values, rather than "numerator=30 and denominator=43."

Detailed Description Text (25):
In the structure shown in FIG. 5, the RGB data in the LCD output circuit 17 are directly transmitted to the data driver 33, and the Hsync signal and the Vsync signal are directly output to the gate driver 31. With this configuration, no special care is required for the PLL of the LVDS. However, if the frequency of the Vclk is lowered while the data driver 33 and the gate driver 31 are performing a drawing process, the transmission of data from the controller 15 to the LCD output circuit 17 is disordered, and as a result, the display contents are disarranged. In the present invention, therefore, the Vclk is changed during the vertical blanking intervals. Since the Hsync signal and the Vsync signal are generated by dividing the frequency of the Vclk using a counter, they can follow the Vclk as long as the Vclk is gradually changed.

Detailed Description Text (29):
Without further analysis, the foregoing provides sufficient information regarding the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting presented features that from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of the present invention, and provide for advantages which include the frequency of the video clock can be changed without the display quality being affected, and that according to the principles of the present invention, the power consumption can be reduced.

CLAIMS:

1. A method for use with a computer display system having an LCD display with a driver having a phase lock loop timed by a video clock of adjustable frequency, said method comprising the steps of: detecting an opportunity which is preselected to initiate a reduction of the frequency of the video clock; lowering the frequency of the video clock in a frequency increment selected to be within a range for which the phase-lock circuit employing the video clock can follow such change in the frequency without loss of stability; and iterating the step of lowering the frequency of the video clock, at least once, until a predetermined frequency is attained.

2. The method according to claim 1, wherein the opportunity which causes the reduction of the video clock is detected in accordance with the type of application whose window is displayed on a screen of the LCD display device.

4. A computer having a LCD display device and a driver which provides an interval between display refreshes and includes a phase-lock circuit which responds to a video clock signal having an adjustable frequency, comprising: signal logic for detecting an operating system execution of certain preselected application programs known to present opportunities for low video activity and signaling such low video activity opportunities; and a controller for lowering the frequency of the video clock to a predetermined frequency during said interval in multiple sub-increments of frequency of a size selected to allow the phase-lock circuit to follow without destabilizing, and for maintaining the predetermined frequency of the video clock until said signal logic signals a change of video activity.

First Hit Fwd Refs

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L3: Entry 27 of 33 File: USPT Aug 18, 1998

DOCUMENT-IDENTIFIER: US 5796391 A
TITLE: Scaleable refresh display controller

Abstract Text (1):
A display controller (112) reduces the power consumed in displaying a graphics image in a portable wireless communications device (100) when a graphics image is smaller than the size of the display (118). The number of rows and columns used to display the graphics image is counted by a decoder (108) which is a microcontroller used to operate the communications device (100). The decoder (108) provides the reduced row or column count to the display controller (112), which reduces the frequencies of clocks (PIXEL CLOCK, LINE PULSE, FRAME PULSE) used for timing data transfers to the display (118). Power is reduced by operating the display (118) at a lower frequency while acceptable frame refresh rates are maintained.

Parent Case Text (2):
The present application is related to copending U.S. patent application, Attorney's Docket No. SC09887C, entitled "DISPLAY DRIVER AND METHOD THEREOF," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,052, by Inventors Scott Chiu and Scott Novis; and patent application, Attorney's Docket No. SC09960C, entitled "NONLINEAR GRAY SCALE METHOD AND APPARATUS," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,055, by Inventors Scott Chiu, Karen Jachimowicz and George Kelly; and assigned to the same assignee, Motorola Inc.

Brief Summary Text (2):
The present application is related to copending U.S. patent application, Attorney's Docket No. SC09887C, entitled "DISPLAY DRIVER AND METHOD THEREOF," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,052, by Inventors Scott Chiu and Scott Novis; and patent application, Attorney's Docket No. SC09960C, entitled "NONLINEAR GRAY SCALE METHOD AND APPARATUS," filed Oct. 24, 1996, U.S. patent Ser. No. 08/740,055, by Inventors Scott Chiu, Karen Jachimowicz and George Kelly; and assigned to the same assignee, Motorola Inc.

Brief Summary Text (4):
The present invention relates in general to display control circuits and more particularly to display control circuits in which the display is scaled down to fit an image.

Brief Summary Text (5):
Wireless communications devices typically receive a transmitted signal which contains information communicated to a user on a display. For example, a pager receives a transmitted signal modulated with digital data in a predefined format. A decoder in the pager is preprogrammed to recognize the predefined format and to perform computations on the digital data for recovering display and control data for operating the display.

Brief Summary Text (6):
The increasing functionality of pagers requires a graphics user interface (GUI) to make pagers easier to program and operate. A GUI includes a display controller which drives a high resolution light-emitting device (LED) display for viewing graphics images such as status icons and downloaded facsimile messages. A typical

LED display is organized into a plurality of rows and columns. An image is displayed by scanning columns and activating rows to illuminate the pixels in the column.

Brief Summary Text (7):
Displaying graphics images requires the display controller to process and transfer large amounts of display and control data. A high frequency clock is needed for transferring data and for maintaining acceptable frame refresh rates for flicker-free display operation. However, high frequencies generate radio frequency interference and increase power consumption in the display and the display controller. The radio frequency interference lowers the performance of a portable wireless communications device while higher power consumption reduces the operating time between battery charges.

Brief Summary Text (8):
Hence a high resolution display controller is needed whose power consumption can be reduced while maintaining flicker-free frame refresh rates.

Drawing Description Text (3):
FIG. 2 is a block diagram of a display controller; and

Drawing Description Text (4):
FIG. 3 shows a display with associated row and column drive circuitry.

Detailed Description Text (2):
FIG. 1 shows a block diagram of a portable wireless communications device 100, such as a pager or cellular telephone. Antenna 102 receives a transmitted radio frequency (RF) carrier signal modulated with digital data in a predefined format, including control data for operating communications device 100 and display data for viewing text and/or graphics images on a display 118. The RF carrier signal is coupled to RF receiver 104 for tuning and amplification. A demodulator 106 receives the amplified RF carrier signal and recovers a baseband digital data stream at its output.

Detailed Description Text (3):
Decoder 108 comprises a microcontroller which is preprogrammed to receive the baseband digital signal and to apply the predefined format to recover video and control components. The video component includes display data comprising a series of eight-bit luminance bytes. Each byte includes two four-bit luminance words which provide information for illuminating two pixels in display 118. The luminance bytes are provided on an eight-conductor bus 120 coupled to a graphics display random access memory (RAM) 110, a row driver 116 and a display controller 112. Although bus 120 is shown as an eight-conductor bus, it should be apparent that data can be provided on a wider or narrower bus as appropriate in a particular embodiment.

Detailed Description Text (4):
The control component includes end-of-line and end-of-frame synchronization signals for reproducing the image on display 118. As the baseband digital signal is processed, decoder 108 counts pixels until an end-of-line synchronization signal is received, thereby computing a pixel count, which represents the number of pixels in a line of the image. Decoder 108 counts lines of the image until an end-of frame signal is received for computing a line count which represents the number of lines in an image frame. The pixel count and line count are provided to display controller 112 on bus 120 accompanied by associated control signals provided on a two-conductor control bus 122. Decoder 108 divides the maximum number of pixels in a line, e.g., 72 pixels per line, by the pixel count to produce a pixel-rate divisor for adjusting the frequency of a PIXEL CLOCK used for timing data transfers on bus 120. Decoder 108 is also programmed to track where image data is stored in graphics display RAM 110 to provide efficient memory utilization.

Detailed Description Text (5):
Decoder 108 performs tasks in communications device 100 not related to displaying images, such as processing downloaded data and interpreting keypad commands. Many display functions are managed by display controller 112, while other control functions are provided by decoder 108. For example, display controller 112 provides incremental memory addresses to graphics display RAM 110 for storing or retrieving downloaded images, but the starting address is provided by decoder 108. A key function of display controller 112 is to minimize power consumption by dynamically adjusting the frequency of data transfers to operate display 118 at the lowest frequency which both reproduces the displayed image and refreshes display 118 at a flicker-free rate. Timing for display controller 112 is provided by a system clock V.sub.SYSTEM operating at a rate of 2.5 megahertz.

Detailed Description Text (6):
Display controller 112 generates a LINE PULSE and a FRAME PULSE on a two-conductor bus 124 which are coupled to column driver 114 for respectively scanning columns and refreshing display 118. A PIXEL CLOCK is produced on bus 126 for clocking display data to row driver 116. A LINE PULSE is generated at bus 126 for resetting row driver 116 to load display data in the first row of display 118.

Detailed Description Text (7):
Graphics display RAM 110 includes an array of read-write storage cells operating as a buffer for storing downloaded display data. Internal images such as status icons which are typically stored in read-only memory (not shown) are also transferred to graphics display RAM 110 for easier accessibility. The timing of transfers of display data to and from graphics display RAM 110 is managed by display controller 112.

Detailed Description Text (8):
Display 118 comprises a matrix of light-emitting devices (LED) such as light-emitting diodes organized into a plurality of rows and columns to operate as pixels of display 118. In one embodiment of communications device 100, display 118 has 72 rows and 120 columns. The cathodes and anodes of the LED pixels are respectively connected to rows and columns in display 118 such that a unique LED pixel is illuminated when a column is selected and a row is activated. Rows and columns are respectively coupled to row and column inputs of display 118.

Detailed Description Text (9):
Column driver 114 has a plurality of outputs coupled to the column inputs of display 118 to operate in a column scan mode in which one column at a time is selected. Successive columns are selected by repetitively clocking column driver 114 with a LIME PULSE. When column driver 114 scans to the last display column of an image, a FRAME PULSE resets column driver 114 to cycle back to the first display column for refreshing display 118.

Detailed Description Text (10):
Row driver 116 has a plurality of outputs which operate in parallel to provide activating pulses to row inputs of display 118 for illuminating LED pixels in the selected column. The activating pulses drive LED pixels to a luminance level determined by four-bit luminance words. Pairs of luminance words are combined into an eight-bit luminance byte and serially clocked into respective pairs of individual cells of row driver 116 by PIXEL CLOCK. When all of the luminance words in a display column have been loaded, display controller 112 issues a LINE PULSE to cycle row driver 116 back to the first pair of cells to load new data.

Detailed Description Text (11):
FIG. 2 shows a block diagram of display controller 112 which is a clocking circuit including latches 202, 208, 212 and 216; programmable dividers 204,210 and 214; an address decoder 206 and an address counter 218. Display controller 112 sets the timing of data transfers among decoder 108, graphics display RAM 110 and row driver

116 in accordance with the size of the displayed image. Timing is varied by dynamically adjusting the frequency of PIXEL CLOCK and the periods of LINE PULSE and FRAME PULSE.

Detailed Description Text (16):
Programmable divider 210 comprises a free-running, four-bit parallel-load down counter. The pixel count is loaded from bus 120 into latch 208 in response to a load signal from address decoder 206, and coupled to a four-bit parallel input of programmable divider 210. Because two luminance words at a time are clocked into row driver 116, the value of the pixel count represents one-half the number of pixels of display data within a column. The pixel count thus ranges in value from 4 to 36. Programmable divider 210 decrements on pulses of PIXEL CLOCK and produces a LINE PULSE upon reaching a zero count. After a LINE PULSE is produced, programmable divider 210 resets to the pixel count and begins the next cycle.

Detailed Description Text (17):
Latch 212 comprises a four-bit parallel-load, parallel output latch which operates in conjunction with programmable divider 214 to control when a FRAME PULSE is generated. A FRAME PULSE resets column driver 114 to select the first column for refreshing display 118. The line count is loaded from bus 120 into latch 212 in response to a load signal from address decoder 206, and coupled to a four-bit parallel input of programmable divider 214. A FRAME PULSE is generated after column driver 114 has successively scanned all of the columns in the displayed image.

Detailed Description Text (19):
Most if not all logic families increase power consumption when the operating frequency increases. The power is typically consumed during logic level transitions when logic gates charge and discharge parasitic capacitances. Additional power is consumed by current spikes which are generated because of delays in turning off transistors in logic gates. When power is consumed at higher frequencies, more RF interference is generated. Besides system clock V.sub.SYSCLK, PIXEL CLOCK operates at the highest dock frequency in communications device 100. Accordingly, PIXEL CLOCK is a source of substantial power consumption when operating at the 1.25 MHz frequency needed for driving display 118 in a full display mode. Smaller images, such as telephone numbers or status icons are fully displayed in fewer rows and columns of display 118 and require fewer data transfers between frame refreshes. If these smaller images are displayed using the maximum 1.25 MHz frequency of PIXEL CLOCK, power is unnecessarily wasted.

Detailed Description Text (20):
The present invention reduces overall power consumption by determining the size of an image and dynamically adjusting clock operating frequencies to transfer data at the lowest frequency that ensures an acceptable refresh rate. For a LED display or other zero persistence display, the minimum refresh rate for flicker-free operation has been determined to be 52.8 hertz. The frequency of PIXEL CLOCK and LINE PULSE are reduced when an image can be displayed with fewer pixels per line, i.e., on fewer rows. The frequency of FRAME PULSE is reduced when the image is displayed using fewer columns. By way of example, for a minimum image size having a square whose dimension is eight pixels on a side, the frequency of PIXEL CLOCK is reduced to approximately (1.25 MHz)/9=137 kilohertz.

Detailed Description Text (21):
Latch 216 comprises an eight-bit parallel-load, parallel output latch which operates in conjunction with address counter 218 to provide addresses to graphics display RAM 110 for storing luminance bytes. The starting address for the first luminance byte is provided by decoder 108 to provide ready access to recently displayed images in order to minimize power consuming data transfers. The starting address is loaded from bus 120 into latch 216 and coupled to address counter 218 by a load pulse from address decoder 206. Successive luminance bytes are stored at incremental addresses generated by address counter 218 in response to PIXEL CLOCK.

Address counter 218 is an eight-bit, parallel-load up counter which has a capacity to generate 256 unique addresses. For images requiring more address space, luminance data can be stored in 256-address pages, where a page address is produced in decoder 108 and coupled on bus 120 directly to graphics display RAM 110.

Detailed Description Text (22):
Referring to FIG. 3, a diagram of display 118 is shown being driven by row and column drivers 116 and 114, respectively. Display 118 comprises a LED matrix coupled to 72 rows and 120 columns to operate each LED as a display pixel. A LED pixel is illuminated when its associated column is selected and its row is driven by an activating signal.

Detailed Description Text (23):
Column driver 114 includes a 120-stage shift register 308 having a feedback output at the last stage coupled to the data input of the first stage to operate shift register 308 as a ring counter. The FRAME PULSE is applied at an input for initializing shift register 308 to produce a column enable signal at the output of the first stage for selecting the first column. The LINE PULSE repetitively applied to the clock input of shift register 308 clocks the column enable signal through successive stages to operate display 118 in a column scan mode.

Detailed Description Text (24):
When display 118 is operating such that all 120 columns are used for displaying an image, shift register 308 operates as a ring counter which shifts the column select signal from the last stage (stage 119) back to the first stage (stage 0) through the feedback output. When the image is displayed on fewer than 120 columns, the FRAME PULSE is produced after the last column has been selected, thereby reinitializing shift register 308 and selecting the first column. For example, if columns 0 through 19 are used for displaying an image, shift register 308 repetitively selects columns 0 through 19. On the next clock cycle, the FRAME PULSE is applied by display controller 112, which initializes shift register 308 and selects column 0 again. Instead of scanning all 120 columns, column driver 114 scans only columns 0-19 needed for displaying the image. The frequencies of the LINE PULSE and FRAME PULSE are therefore reduced accordingly. In an alternative embodiment, shift register 308 includes parallel inputs which load data representative of a starting column in response to the FRAME PULSE to display an image at any column of display 118.

Detailed Description Text (27):
Row driver cell 304 has an output coupled to a row input of display 118. The output provides an activating signal for illuminating a LED pixel in the selected column. Row driver cell 304 comprises a flip-flop which is clocked by the LINE PULSE to load a luminance bit and initiate the activating signal as determined by the value of the luminance bit. Alternatively, gray scale pixel shading is provided by a digital-to-analog converter (not shown) whose output provides the activating signal having an amplitude determined by the value of the luminance word. The amplitude of the activating signal defines a current in the LED pixel for producing a variable luminance.

Detailed Description Text (30):
In full display mode, 36 pulses of PIXEL CLOCK increment row address counter 302 to count row addresses from 0-35. Where the image size is reduced, a LINE PULSE reinitializes row address counter 302 to a zero count after loading a luminance word into the last row of the displayed image. For example, if an image is displayed using 40 rows, i.e., 20 row addresses, then row address counter 302 counts from 0-19 and a LINE PULSE reinitializes row address counter 302 back to a 0 count.

Detailed Description Text (31):
The present invention thereby provides a display controller for displaying a

graphics image in a portable wireless communications device which operates at a reduced power level. The number of rows and columns in the displayed graphics image is counted by a decoder, which provides line and frame counts to the display controller for adjusting the period of a LINE PULSE and a FRAME PULSE to correspond to the image size. The decoder produces a pixel-rate divisor which is loaded into a binary counter in the display controller to reduce the frequency of the PIXEL CLOCK when fewer data transfers are needed to display the image.

Detailed Description Text (32):
By continuously monitoring the number of rows and columns in the displayed image, the present invention is able to dynamically adjust the PIXEL CLOCK, LINE PULSE and FRAME PULSE frequencies to the lowest value which allows the image to be displayed without display flicker. The reduced frequency operation reduces the power consumed by column driver 114 and row driver 116 during logic level transitions resulting from current spikes in the logic gates and the charging and discharging of parasitic voltages. Besides extending battery operating time, the reduced frequencies improve the performance of the portable wireless communications device by reducing RF interference.

CLAIMS:

1. A wireless communications device for viewing an image on a display, comprising:

a radio frequency (RF) circuit having an input coupled for receiving a RF input signal and an output;

a demodulator having an input coupled to the output of the RF circuit and having an output for providing a baseband data signal;

a decoder circuit having an input for receiving the baseband data signal for providing image data, where the decoder circuit counts a number of pixels within a line of the image data to produce a pixel count and divides a number of pixels within a line of the display by the pixel count to compute a pixel rate divisor;

a circuit for clocking the display, including

(1) a first divider having a clock input for receiving a clock signal, a data input for receiving the pixel rate divisor, and an output for providing a pixel clock for transferring the image data to the display; and

(2) a second divider having a clock input for receiving the pixel clock, a data input for receiving the pixel count, and an output for providing a line clock having a substantially constant period as a period of the pixel clock varies.

2. A clocking circuit for driving a display device, comprising:

a decoder circuit having an input for receiving a data stream and an output for providing image data, the decoder circuit counting a number of pixels within a line of the image data to produce a pixel count and dividing a number of pixels within a line of the display device by the pixel count to compute a pixel rate divisor;

a first divider having a clock input for receiving a clock signal, a data input for receiving the pixel rate divisor, and an output for providing a pixel clock for transferring the image data; and

a second divider having a clock input for receiving the pixel clock, a data input for receiving the pixel count, and an output for providing a line clock having a substantially constant period as a period of the pixel clock varies.

10. A method of clocking a display, comprising the steps of:

counting a number of pixels within a line of the image data to produce a pixel count;

dividing a number of pixels within a line of the display by the pixel count to compute a pixel rate divisor;

counting a system clock to the pixel rate divisor to produce a pixel clock for transferring the image data; and

counting the pixel clock to the pixel count to produce a line clock having a substantially constant period as a period of the pixel clock varies.